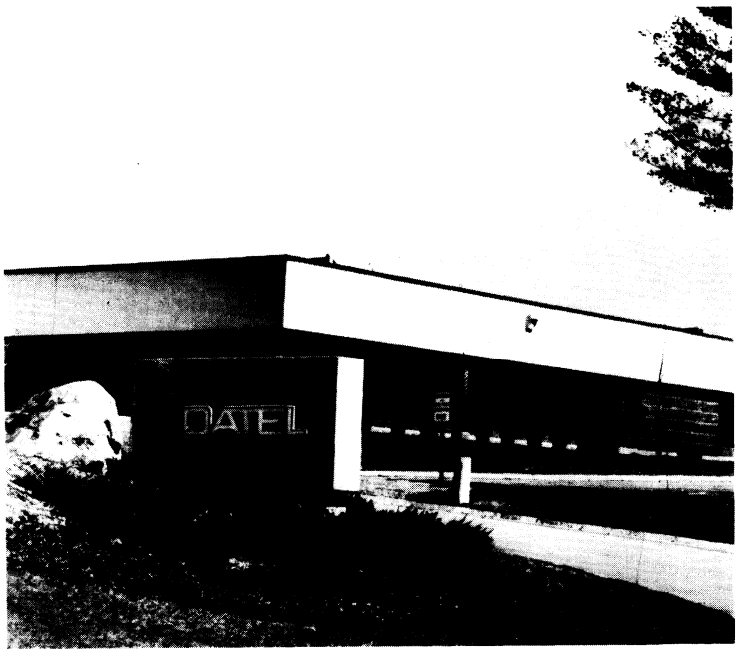
DATEL

DATA ACQUISITION BOARDS

INNOVATION AND EXCELLENCE IN
PRECISION DATA ACQUISITION

COMPANY HISTORY



DATEL is a leader in high performance data acquisition products including components, subsystems, power supplies, and instruments. The privately-held corporation is a multinational company founded in 1970. Our modern 180,000 square foot facility houses administrative offices, manufacturing, and design groups.

Our worldwide sales and support group includes direct all-DATEL subsidiaries and authorized representatives. The people who implement this network are skilled professionals dedicated to providing the highest level of quality and service.

ABOUT THIS CATALOG

These products show DATEL's high performance data conversion components efficiently integrated into fast, bus-compatible boards for popular VMEbus, Multibus, PC, and PC/AT busses. These boards emphasize user configurability for a wide range of applications. The architecture on these boards is the result of years of evolution in interface design, constant testing with real-world operating systems, sensors of all kinds, all popular computer languages, and extensive experience assisting customers. For the majority of applications, these designs represent the best blend of cost, function, performance, expandability, host compatibility, and programming ease.

DON'T DESIGN IT YOURSELF!

Modern system interface design is not trivial. Busses are very fast (they act like RF transmission lines), and today's cached virtual-memory microprocessors are complex miniature subsystems. Getting all the performance possible out of a high speed A/D converter is challenging. We know from experience! Adding sensor noise and nonlinearity, math throughput, disk and display delays demand high performance from every aspect of the system. Achieving low harmonic noise, ease of programming, and manufacturability are difficult tasks for today's board designer. It's hard to be an expert on all parts of a board project. DATEL uses a team of designers with many skills. Take a look at these cost-effective products and don't design it yourself!

QUALITY IS DESIGNED IN

The heart of any A/D - D/A system is the signal quality and performance inherent in the components. Unlike many other board manufacturers, DATEL builds the high performance data acquisition components in our hybrid microcircuit facility. We control all aspects of product quality from the internal resistor networks through vendor screening to manufacturing test software. This is the same MIL-STD-1772 qualified facility supplying fully militarized converters for defense, avionics, and space applications.

A WORD ABOUT OUR PRODUCTS

For additional support, customers may consult our Application Engineering Department. Experienced engineers will answer questions about the products and offer advice on how to fulfill your goals.

AVAILABLE LITERATURE

DATEL'S ALL NEW DATA ACQUISITION HANDBOOK SERIES

The following additional Handbooks are presented in complete data sheet format and include Selection Guides, Application Notes, and Ordering Information.

Volume 1. Components
ADS, ADC, DAC, SHM, HDAS, MUX, AM

Volume 3. Industrial Monitor and Control Products
Process Monitors, Digital Panel Meters, Thermal Panel Printers, Benchtop and Hand-held Calibrators

Volume 4. Power Products
DC/DC Converters, Power Supplies

Also available are the following Application Notes:

AN-1 High-Speed A/D Converter Designs: Layout and Interfacing Pitfalls

AN-2 Picking the Right Sample-and-Hold Amp for Various Data Acquisition Needs

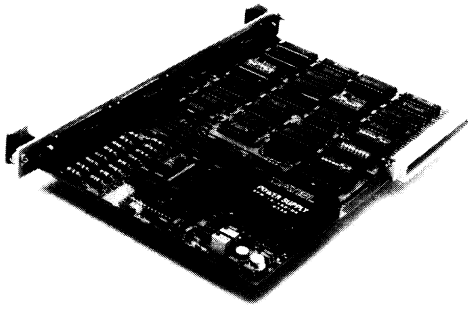
AN-3 Data Converters: Getting to Know Dynamic Specifications

Data Acquisition and Conversion Handbook:
A technical guide to A/D - D/A converters and their applications

Exciting New VMEbus Products

DVME-613

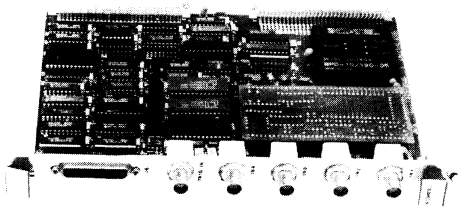
Protected, Isolated Analog Inputs for Control
and Measurement Applications



- 16S or 8D analog inputs, 500 Volt isolation
- Direct sensor connection using programmable gain amplifier
- On-board start timer and vectored interrupt generator
- Discrete digital I/O, 8 in/8 out
- Includes "C" program disk for any OS
- Low cost per channel

DVME-614

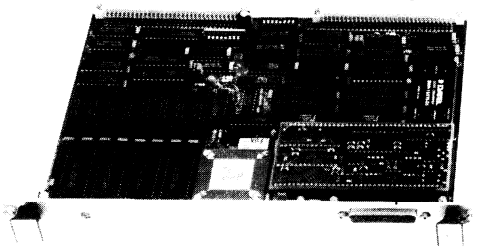
High-Speed Analog Input
for DSP, Array Processors, and FFT's



- Up to 4 MHz A/D sample rate
- Choice of 12- or 14-bit A/D resolution
- 4 channel simultaneous sample/hold's (optional)
- Very low harmonic distortion
- Non-bus parallel burst data outport for "seamless" non-stop recording
- FIFO memory, analog comparator trigger

DVME-630

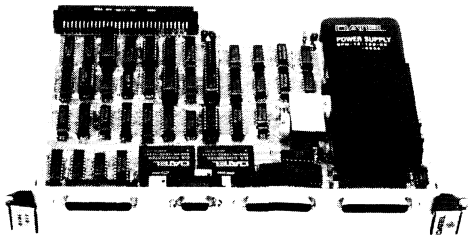
Very High Speed A/D-DSP
Coprocessor with Resident DSP Library



- Up to 4 MHz A/D sample rate
- Choice of 12- or 14-bit A/D resolution
- On-board 320C30 32 MHz Digital Signal Processor, 128K x 32 Dual Port RAM
- Fast, easy-to-use, powerful command Executive (no local programming)
- DSP Software Library includes FFT's, windowing, filters, floating point, non-stop sampling, etc.

DVME-611F/-612F

Fast, Low-Cost, 14-bit A/D Input
for Multichannel Instrumentation

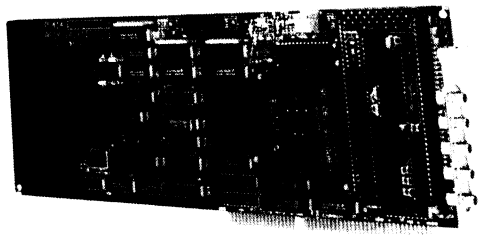


- 32S or 16D analog inputs, 14-bit resolution
- Up to 250 KHz sampling (single channel)
- Software Programmable Gain Amplifier
- Two analog output channels optional
- Channel expansion up to 256 channels
- Vectored VMEbus interrupts. Trigger input
- Simple programming for any Operating System

New High Performance Boards and Software for PC's and AT's

PC-414

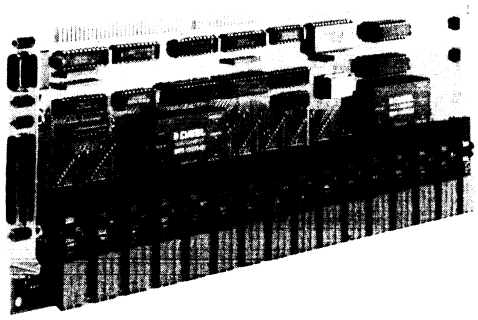
High Speed Analog Input
for DSP, Array Processors, and FFT's for PC/AT's



- Up to 4 MHz A/D sample rate
- Choice of 12- or 14-bit A/D resolution
- 4 channel simultaneous sample/hold's (optional)
- Very low harmonic distortion
- Non-bus parallel burst data outport for "seamless" non-stop recording
- FIFO memory, analog comparator trigger
- Windowed setup/configuration data save software

PC-422

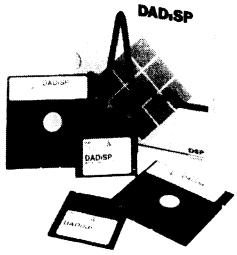
8- or 16-Channel Fast Simultaneous
Analog Output Board for IBM-PC/AT's



- 12-bit D/A resolution
- 3 microseconds settling time
- Simultaneous update of all channels
- Trigger timer interrupt
- Digital I/O (4 in/4 out)
- Output ranges selectable per channel
- Software selected trigger timer
- Ideal for coherent waveform generation

PC-DADiSP

Comprehensive Math, DSP
and Display Software for Analog Input Boards



- Over 300 graphics and math functions
- Comprehensive DSP and FFT processing
- "No programming" pop-up windows and menus for ease of use
- Accepts analog signal files limited only by disk size
- Powerful macros to customize your application

PC-411/412

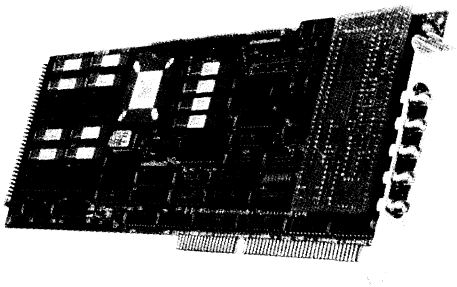
16-Channel Analog I/O Board
with FIFO for IBM-PC Computers

- 16S or 8D signal conditioned analog inputs
- 4 analog output channels optional with simultaneous update
- Choice of 12- or 14-bit A/D resolution
- PGA, timer trigger, interrupt and DMA
- Discrete digital I/O (8 in/ 8 out)
- FIFO memory for non-stop streaming to disk
- Ideal for process control, labs and ATE
- Low cost per channel

New High Performance Boards and Software for PC's and AT's

PC-430

Very High Speed A/D-DSP Coprocessor
with Resident DSP Library



- Up to 4 MHz A/D sample rate
- Choice of 12- or 14-bit A/D resolution
- On-board 320C30 32 MHz Digital Signal Processor, 128K x 32 Dual Port RAM
- Fast, easy-to-use, powerful command Executive (no local programming)
- DSP Software Library includes FFT's, windowing, filters, floating point, non-stop sampling, etc.

PC-430HYPER

Fully Integrated Disk-streaming DSP
and Display Software for the PC-430

- Collects data to hard disk at up to 150,000 samples per second
- Simultaneous DSP processing, graphics display and disk save
- Real time spectrum analyzer and digital oscilloscope
- 3D FFT "waterfall" spectrogram (spectral history display)

PRODUCT INDEX

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- **Power Supplies**

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for
Immediate Assistance

Data Acquisition Boards for PC/XT/AT/EISA Bus

PC/AT A/D-D/A BOARDS

Model	A/D Channels	A/D Resolution	A/D Speed	Prog. Gain Amplifier	In/Out Ranges	D/A Channels	D/A Resolution	Notes
PC-414A	4 SE w/simul sampling	12 Bits	1.5 MHz	x1 or x10	5V, 10V, 1V	1	12 Bits	4K-sample FIFO memory, analog trigger, parallel data port, counter/timer, DMA Vectored interrupt
PC-414B	4 SE	14 Bits	500 KHz	---	5V, 10V	1	12 Bits	
PC-414C	4 SE	12 Bits	1 MHz	---	5V, 10V	1	12 Bits	
PC-414D	1 SE	12 Bits	4 MHz	---	1V	1	12 Bits	
PC-414E	16 SE	12 Bits	400 KHz	x1 to x100	10V to 100 mV	1	12 Bits	
PC-430A	4 SE w/simul sampling	12 Bits	1.5 MHz	x1 or x10	5V, 10V, 1V	None	---	Local 32 MHZ 320C30 DSP, 512K memory,DMA Fast "no prgmg" command executive, DSP library, Vectored interrupt
PC-430B	4 SE	14 Bits	500 KHz	---	5V, 10V	None	---	
PC-430C	4 SE	12 Bits	1 MHz	---	5V, 10V	None	---	
PC-430D	1 SE	12 Bits	4 MHz	---	1V	None	---	
PC-430E	16 SE	12 Bits	400 KHz	x1 to x100	10V to 100 mV	None	---	

PC-411, PC-412
16-Channel Analog I/O Board with FIFO for IBM-PC Computers

FEATURES

- **16S or 8D analog input channels**
- **4 Analog output channels optional (PC-412) with simultaneous update**
- **Choice of 12 or 14 bit A/D resolution**
- **FIFO memory, DMA, and programmable interrupts for continuous, non-stop "streaming" data acquisition**
- **Programmable gain amplifier**
- **On-board programmable trigger clock**
- **Discrete digital I/O (8 input, 8 output)**

GENERAL DESCRIPTION

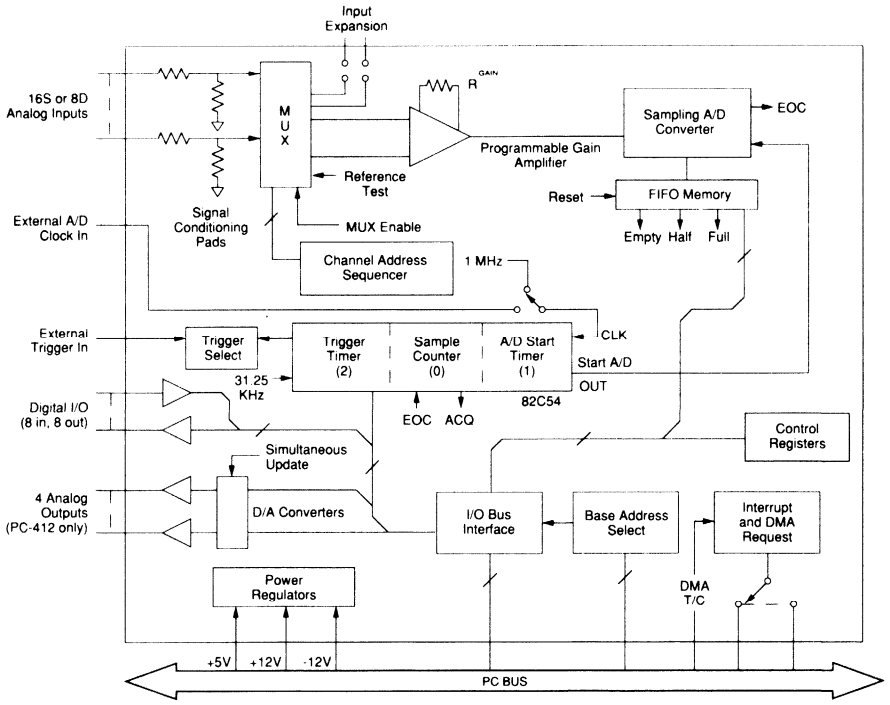
Offering non-stop continuous collection of up to 16 analog input signals in real time, the PC-411 is an analog input board for IBM-PC, PC/XT, PC/AT, and compatible computers. The PC-411 accepts 16 single-ended or 8 differential input signals, digitizes them up to 12- or 14-bit resolution and places them on the computer bus under software control. Data may then be stored in PC memory, saved on disk or displayed on the screen or printer.

Model PC-412 is a combination analog input and output board using the same input section as the PC-411. The PC-412 adds four optional analog output channels to be used for chart recorders, actuator controllers or other output devices. Both the PC-411 and -412 accept external analog input expansion channels. On both the 411 and 412, sixteen discrete digital I/O lines are configured as 8 inputs and 8 outputs for external logic devices.

The digital outputs can control the channel addressing of an expansion input multiplexer. The differential analog inputs offer rejection of common mode noise while the on-board Programmable Gain Amplifier (PGA) offers higher gains (up to times 100) for low level sensors. On-board circuit pads may be configured for other input voltage or current ranges or input signal conditioning.

Analog to digital converter (A/D) data passes to an on-board First-In, First Out (FIFO) data memory. FIFO data is then transferred to the host computer bus interface under software control. Besides temporarily storing a block of samples, the FIFO acts to decouple the precise timing of the A/D section from the block-oriented data transfer burst on the bus.

Unlike many other analog input boards for the PC, the PC-411/412 can continuously collect analog data with non-stop converter triggering while data is simultaneously read by the PC from the FIFO. This allows the collection of "seamless" signals of millions of samples or greater. Another advantage of the FIFO is high speed disk recording of analog data with no loss of samples during disk writes.



PC-411/412 Block Diagram

The timing section controlling the sampling A/D converter is designed for accurate multi-scan data acquisition. Software programmable timers control the interval between each conversion and each multichannel scan. A programmable sample counter will allow sample blocks of specified length independent of FIFO length. The timer/counter section uses an internal clock or an external timebase. The external trigger may be used to precisely synchronize sampling with external events. The trigger may start a single sample, a single multichannel scan, or "N" multiple scans separated by programmable delays.

Either an interrupt, DMA Request, or status flag indicates when FIFO data is ready. Normally, a FIFO interrupt from the PC-411/412 triggers the PC to burst a fixed-length block of samples to host PC memory. This offers very high overall system speed by not tying up the bus and allows the PC to continue with graphics, math, or disk activities.

The PC-412 analog output channels include a simultaneous update option where all channels drive their outputs to new values at the same time from a software trigger. Applications for this include phase-synchronous system simulation, process control, and coherent field waveform generation.

Many options are software configured, reducing the number of jumpers required. Software is available on MS-DOS disks to configure the board and save data. A comprehensive user's manual is also included.

FUNCTIONAL SPECIFICATIONS

(Typical at +25 °C, dynamic conditions, G = 1, unless noted)

ANALOG INPUTS	
Number of Channels (software-selectable)	16 single-ended or 8 differential channels
Input Channel Expansion	External differential analog inputs may be accepted to add additional input channels. Input characteristics are identical to the on-board inputs.
Input Configuration	Non-isolated
Full Scale Input Ranges (gain = 1)	0 to +5V, ±5V (software-selectable). Other voltage and current ranges are available with user-installed precision resistors.
Input Impedance	100 Megohms, power on, 1.5 Kilohms, power off.
Input Bias Current	±200 pA
Input Capacitance	15 pF per channel
Input Overvoltage	±12V max. (no damage)
Overvoltage Recovery Time	5 microseconds
Common Mode Voltage Range	±5V to analog common
Common Mode Rejection	80 dB, dc to 60 Hz, gain = 100
Programmable Gain Amplifier	1 to 100 gains, selectable by precision gain resistor (pads provided).
PGA Settling Delay	6 µSec. to 0.01% (gain = 1) 15 µSec. to 0.02% (gain = 10) 80 µSec. to 0.1% (gain = 100)
A/D CONVERTER	
Resolution	12 bits (PC-411/412A) 14 bits (PC-411/412B)
A/D Conversion Period	12 microseconds (PC-411/412A) 14 microseconds (PC-411/412B)
Aperture Time	25 nanoseconds
Acquisition Time	3 microseconds
Output Coding	Positive-true left-justified straight binary (unipolar) or offset binary (bipolar).
Trigger Sources (software selectable)	1. Local Pacer sample clock 2. External digital sample clock
Addressing Modes	1. Single channel 2. Sequential with autosequenced addressing 3. Random addressing by host software
INPUT SYSTEM PERFORMANCE	
Integral Nonlinearity	±0.05% of FSR (PC-411/412A) ±0.015% of FSR (PC-411/412B)
Differential Nonlinearity	±0.5 LSB
Full Scale Temperature Coefficient	±0.1 LSB per °C (PC-411/412A) ±0.3 LSB per °C (PC-411/412B)
Zero or Offset Temperature Coefficient	±0.1 LSB per °C (PC-411/412A) ±0.3 LSB per °C (PC-411/412B)
Monotonicity	No missing codes
Power Supply Rejection	±0.01% of PC bus ±12V
Total Scan Throughput (sample-to-sample with sequential addressing)	20 microseconds (PC-411/412A) 23 microseconds (PC-411/412B) (see Notes)
Total Throughput (no channel advance)	15 microseconds (PC-411/412A) 17 microseconds (PC-411/412B)
A/D MEMORY	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	256 A/D Samples
TRIGGER CONTROL	
Programmable Timer/Counter Type	82C54
Functions	1. EOC sample count 2. A/D start rate (16 bit divisor) 3. Scan or frame rate (16 bit divisor)
Sample Counter	1 to 65,536 samples. Drives the Acquire flag/interrupt
A/D Start Clock Source (software programmable)	Internal crystal clock. Range 500 KHz to 15.26 Hz (16-stage binary divider or BCD).
Trigger Source (user-selectable)	1. Internal crystal clock 2. External digital input. TTL levels, triggers on rising edge.
Internal Trigger Range (software programmable)	15.625 KHz to 4.19 seconds (16-stage binary divider or BCD)
ANALOG OUTPUT	
Number of Channels	4 channels, single-ended
Resolution	12 bits
Output Voltage Range	0 to +5V, ±5V, jumper selectable per channel
Output Current	±5 milliamps, short circuit protected.
Nonlinearity	±0.05% of FSR
Settling time (full scale step)	5 microseconds to 0.05% of FSR
Input Coding	Same as input section
Temperature Coefficients	Same as input section

PC BUS INTERFACE	
Architecture	Decodes 16 byte-wide I/O registers using address lines A9-A0. Highest base address is 3F0h.
Data Bus Width	8 bits.
PC Bus Interrupt (software maskable)	1 line. Software selectable IRQ 3, 5, 7.
Bus Interrupt Sources	Scan acquire flag (sample count). FIFO full, half full or not empty or DMA T/C.
Bus Data Transfer Rate	1 Megabyte/second or greater. Dependent on host PC CPU speed.
Direct Memory Access	1 line, software selectable, DRQ1 or DRQ3 from FIFO HF, FF, EF* or ACQ.
PARALLEL PORT	
Parallel Outport	8 lines, TTL levels. 2 mA out
Parallel Inport	8 lines, TTL levels, 24 mA in plus pullup resistor to +5V
CONNECTORS	
Analog Inputs, P1	25-pin female DB-25S connector on rear mounting bracket for analog inputs and trigger.
Analog Outputs, P2 (PC-412 only)	9-pin female DB-9S connector on rear mounting bracket.
Parallel Port	Internal header connector, 0.025 inch pins on 0.100 inch spacing, suitable for flat cable.
PC Bus Connector	Edgeboard connector
MISCELLANEOUS	
Power Required (PC-411)	+5V dc, ±5% at 1.0 Amps max. and ±12V dc, ±5% at 100 mA max. all supplied from the bus.
(PC-412)	+5V: 2.0 Amps. max. ±12V: 250 mA max.
Operating Temperature Range	0 to +60 °C Forced cooling is recommended.
Storage Temperature Range	-20 to +80 °C
Relative Humidity	10% to 90%, non-condensing.
Altitude	0 to 10,000 feet.
Outline Dimensions	4.2" H x 13.31" L x 0.625" D (11,43 x 33,81 x 1,59 cm) compatible to PC bus.
Weight	10 ounces (290 grams)
Analog Section Adjustments	Inputs: offset and gain Outputs: offset and gain per channel.

NOTES/DEFINITIONS

Input Settling Delays:

The PC-411/412 will run faster in single channel operation than multichanel after the input is settled on the first channel. Total sample-to-sample throughput time must include input multiplexer settling time after changing the channel address, PGA settling time (depending on the gain), sampling A/D converter acquisition time, and A/D conversion time. The PC-411/412 sampling rate will not be delayed by FIFO-to-PC data transfers if the FIFO is not full.

Sampling Rate per Channel

The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling delays. For example, if four channels were scanned, the maximum sample rate on any one channel of the PC-411/412 would be 20 microseconds times 4 channels, equalling 80 microseconds (12.5 KHz per channel). Observe Nyquist sample rate rules for inputs with unknown spectral content.

To avoid overload recovery delays, do not let the analog input exceed the input voltage range.

Highest total system speeds will be achieved if the FIFO is block transferred using DMA or the REP INS instruction in a loop with the CX register controlling the count of samples transferred.

Scan:
A group of channels sampled together with equal delays between each A/D sample, set by the A/D start clock. A scan is 16S or 8D channels or less. A scan uses sequential channel addressing.

Frame:
One or more channels sampled together at each trigger with equal delays between each A/D sample, set by the A/D start clock. Each frame is started by one trigger. Either single channel or autosequential scan addressing may be used. A frame may consist of several contiguous scans with wrap around addressing. Frames are stopped when the counter 0 Acquire bit is reset to zero.

PROGRAMMING

(Refer to the PC-411 user manual for detailed programming information.)

The BASE address may be selected anywhere up to 3F0h on 16-byte boundaries. At power up or PC bus reset, all registers contain zeroes except the FIFO HF and FF bits. When setting one bit in a write only register, remember to select all other bits according to the desired code. A shadow register should be considered to store the last value written. The registers may be programmed in any sequence as long as the command register is last. "x" bits are don't care or not used.

I/O REGISTER MAPPING

I/O Address (Hex)	Direction	Description
BASE + 0	Write	Command Register
BASE + 0	Read	Status Register
BASE + 1	Write	Channel Address Register
BASE + 1	Read	FIFO A/D Data Register
BASE + 2	Write	Interrupt/DMA Register
BASE + 2	Read	FIFO Reset Register
BASE + 3	Write	Digital Output Port
BASE + 3	Read	Digital Input Port
BASE + 4	Read/Write	Counter #0 (82C54)
BASE + 5	Read/Write	Counter #1 (82C54)
BASE + 6	Read/Write	Counter #2 (82C54)
BASE + 7	Read/Write	Control Word (82C54)
BASE + 8	Write	DAC 0 low byte
BASE + 9	Write	DAC 0 high byte
BASE + 10	Write	DAC 1 low byte
BASE + 11	Write	DAC 1 high byte
BASE + 12	Write	DAC 2 low byte
BASE + 13	Write	DAC 2 high byte
BASE + 14	Write	DAC 3 low byte
BASE + 15	Write	DAC 3 high byte

COMMAND REGISTER (Write BASE + 0)

7	6	5	4	3	2	1	0
A/D Calib	Chan Expnd	Read A/D Ref	SE/ Diff	Unipolar or Bipolar	Auto Incr	A/D Conv Enbl	Trig Int/ Ext

Internal/External Select [Bit 0]
0 = Internal trigger from 82C54 timer 2.
1 = External digital trigger

A/D Converter Enable [Bit 1]
0 = Disable A/D conversion
1 = Enable A/D conversion

Both the command bit 1 and the counter 0 ACQuire gate must be set to enable A/D conversions.

Channel Address Autoincrement [Bit 2]
0 = Single channel (no increment)
1 = Sequence channel address after A/D conversion.

In autoincrement, the channel address advances on the A/D EOC rising edge. For continuous scanning, the address wraps around to channel 0 after reaching channel 15, modulo 16. Eight-channel boards wrap after channel 7. Allow adequate settling time before starting the next A/D conversion. In single channel mode, the A/D may be triggered as fast as the EOC appears.

Unipolar/Bipolar [Bit 3]
0 = A/D input range is 0-5V.
1 = A/D input range is ±5V.

Single-ended/ Differential [Bit 4]
0 = Input configuration is single-ended, 16 channels.
1 = Input configuration is differential, 8 channels.

Read A/D Reference [Bit 5]
0 = Normal input sampling
1 = Select reference input

This bit selects a +4.5V dc reference channel on the A/D converter to verify A/D operation. It is not used for calibration.

Input Channel Expansion [Bit 6]
0 = Enable local channels, disable expansion inputs.
1 = Disable local channels, enable expansion inputs.

Bit 6 switches a downstream multiplexer between the local channel multiplexer and the differential expansion input channel. If an external user-supplied multiplexer is used for expansion channels, control external channel addressing using the parallel digital outputs.

Calibrate A/D Converter [Bit 7]
0 = Normal operation
1 = Start calibration cycle

Writing a one to this bit then resetting it back to zero begins an A/D linearization sequence. This takes approximately 20 milliseconds until EOC. Perform this operation once after power up. During calibration, the A/D converter makes internal corrections. Periodic calibration is optional in stable temperature environments but is suggested frequently with significant temperature changes.

STATUS REGISTER (Read BASE + 0)

7	6	5	4	3	2	1	0
End of Conv	FIFO Full*	FIFO Half Full*	FIFO Empty*	Acquire Status	Auto Incr Enbl	A/D Conv Enbl	Trig Int/ Ext

Bits 0, 1, and 2 echo the corresponding control register bits and verify proper register loading.

Acquisition Status [Bit 3]
0 = A/D scan not in progress or scan is done. (Counter 0 EOC sample count was reached). The A/D is disabled.
1 = A/D scan in progress.(Counter 0 EOC sample count was not reached).

The ACQuire bit resets to zero after a fixed number of samples (up to 65,536) have been transferred to the FIFO. The sample count is set by Counter 0. The A/D start clock is inhibited when ACQ is 0. A special mode allows continuous non-stop A/D triggering for frames larger than 65K.

FIFO Memory Status Flags
Bit 4: 0 = FIFO is empty, 1 = FIFO is not empty.
Bit 5: 0 = FIFO is half full or greater. 1 = FIFO is less than half full.
Bit 6: 0 = FIFO is full, 1=FIFO is not full.

*Note the negative true coding on these bits.

End of A/D Conversion Status (EOC)[Bit 7]
0 = A/D conversion in progress, data is invalid.
1 = A/D conversion is done, data is ready.

Note that all data transfer is through the FIFO. EOC is used only to monitor the A/D converter. EOC is reset to zero by the next A/D start convert clock. EOC clocks A/D data into the FIFO.

INPUT CHANNEL ADDRESS REGISTER (Write BASE + 1)

7 - 4	3 2 1 0
Not Used	Start Channel Address

Start Channel Address [Bits 3-0]

In single channel mode, these bits select the address of the next input channel for A/D conversion.

In autoincrement mode, bits 3-0 are the starting channel address. After each A/D conversion, the EOC automatically sequences the address. The address wraps around to channel 0 after reaching channel 15 in single-ended mode or channel 7 in differential mode. If an exact multiple of 8D or 16S channels is triggered, and the user's program counts samples, the channel address will not need reloading. The user must count samples read from the FIFO to determine the current channel address or must periodically reload the starting address.

For either single channel or autoincrement, allow adequate settling time after changing the address before starting the next A/D conversion.

FIFO A/D DATA REGISTER (Read BASE + 1)

First Read:

7	6	5	4	3	2	1 - 0
AD 9	AD 10	AD 11	AD 12	AD 13	AD 14	Not Used
			LSB 12		LSB 14	

Second Read:

7	6	5	4	3	2	1	0
AD 1	AD 2	AD 3	AD 4	AD 5	AD 6	AD 7	AD 8
MSB ALL							

12 or 14-bit A/D data is presented in two sequential reads at the same output port location. The least significant byte is read first. The data is left justified and unused least significant bits are zeroes. Note that A/D data assigns the MSB as A/D bit 1. For bipolar inputs, the MSB indicates polarity (0=negative, 1=positive).

INTERRUPT CONTROL REGISTER (Write BASE + 2)

7	6	5 4	3 2	1 0
Simultaneous Update DAC	Not Used	DMA Level 1 0	Interrupt Level 1 0	Int/DMA Source 1 0

Hardware flags in the PC-411/412 may cause either an interrupt or a DMA request. If both an interrupt and DMA are enabled, an interrupt will be generated by the PC bus DMA Terminal Count signal. For fast block transfers with no host PC polling overhead, start a DMA block transfer at the FIFO half full flag. Immediately after the DMA starts, reconfigure the interrupt system to indicate from the DMA T/C interrupt when the block is done. After the T/C, reconfigure to the HF DMA mode again then process the previous DMA buffer.

Interrupt or DMA Source

Bits 1 0
- 0 0 = Interrupt or DMA request at FIFO full flag.
- 0 1 = Interrupt or DMA request at FIFO half full flag.
- 1 0 = Interrupt or DMA request at Data Acquire flag. Counter 0 EOC sample count reached.
- 1 1 = Interrupt or DMA request at FIFO not empty flag.

This last mode will allow single A/D samples to cause an interrupt or DMA request.

Interrupt Level

Bits 3 2
- 0 0 = Interrupt disable
- 0 1 = Interrupt request on the IRQ 3 line
- 1 0 = Interrupt request on the IRQ 5 line
- 1 1 = Interrupt request on the IRQ 7 line

DMA Level Select

Bits 5 4
- 0 0 = DMA disable
- 0 1 = DMA request on DRQ 1 line
- 1 0 = DMA request on DRQ 3 line
- 1 1 = Spare

Only block mode DMA transfers are available (no single samples).

Simultaneous DAC Update [Bit 7]
- 0 = Writing to a DAC high byteregister will update that channel.
- 1 = All DAC's will simultaneously update when bit 7 is toggled to zero then back to one.

If bit 7=1, writing to a DAC will not update that channel but data will be stored for later simultaneous update.

FIFO MEMORY RESET REGISTER (Read BASE + 2)

7 - 0
x - x

Reading this register clears the FIFO and sets the empty flag true. All previous FIFO data is lost. If A/D conversion is still running, the FIFO will not be empty when the next A/D EOC occurs.

DIGITAL OUTPORT REGISTER (Write BASE + 3)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0

Discrete digital outputs are loaded in these bits.

DIGITAL INPORT REGISTER (Read BASE + 3)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0

Discrete digital inputs are read in these bits.

82C54 PROGRAMMABLE INTERVAL TIMER

Counter Register
- (Read/Write BASE + 4 - Counter #0)
- (Read/Write BASE + 5 - Counter #1)
- (Read/Write BASE + 6 - Counter #2)

7	6	5	4	3	2	1	0
C07	C06	C05	C04	C03	C02	C01	C00

Counter 0 counts up to 65,536 A/D samples (load one less than the desired number of samples). Counter 0 inhibits A/D conversions when the count is reached. It automatically reloads the sample count at the next trigger. A special method is available for non-stop continuous sampling beyond 65K samples (select mode 4 and DO NOT write the counter registers).

Counter 1 determines the A/D clock rate using a 1 MHz clock.

Counter 2 determines the internal trigger rate between scans or data frames using a 31.25 KHz clock.

Control Word Register (Read/Write BASE + 7)

7	6	5	4	3	2	1	0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Select Counter

SC1	SC0	
0	0	Select counter #0
0	1	Select counter #1
1	0	Select counter #2
1	1	Read back command

Read/Load

RL1	RL0	
0	0	Counter latch operation
0	1	Read/Load LSB only
1	0	Read/Load MSB only
1	1	Read/Load LSB then MSB

Mode

M2	M1	M0	
x	1	0	Mode 2 rate generator
1	0	0	Mode 4 software strobe
1	0	1	Mode 5 hardware strobe

BCD

BCD	
0	16-bit binary count
1	4-decade binary coded decimal count

DAC 0 LOW BYTE (Write BASE + 8)
DAC 1 LOW BYTE (Write BASE + 10)
DAC 2 LOW BYTE (Write BASE + 12)
DAC 3 LOW BYTE (Write BASE + 14)

7	6	5	4	3 2 1 0
DA 9	DA 10	DA 11	DA 12 LSB	Not Used

DAC 0 HIGH BYTE (Write BASE + 9)
DAC 1 HIGH BYTE (Write BASE + 11)
DAC 2 HIGH BYTE (Write BASE + 13)
DAC 3 HIGH BYTE (Write BASE + 15)

7	6	5	4	3	2	1	0
DA 1 MSB	DA 2	DA 3	DA 4	DA 5	DA 6	DA 7	DA 8

DAC data is left justified. With the ±5 Volt bipolar output range, the MSB is used for polarity (0=negative, 1=positive).

In single-channel mode (B + 2 bit 7 = 0), write the high byte last to update all DAC bits.

A/D CODING TABLE

Input (unipolar)	Input (bipolar)	Output Code (Hex)
+Full scale -1 LSB	+Full scale -1 LSB	FFF0h
1/2 FS +1 LSB	+1 LSB	8010h
1/2 full scale	Zero	8000h
1/2 FS -1 LSB	-1 LSB	7FF0h
Zero	-full scale	0000h

Pin numbering is shown as viewed from rear panel. (Channel addresses use the notation, single-ended/differential.)

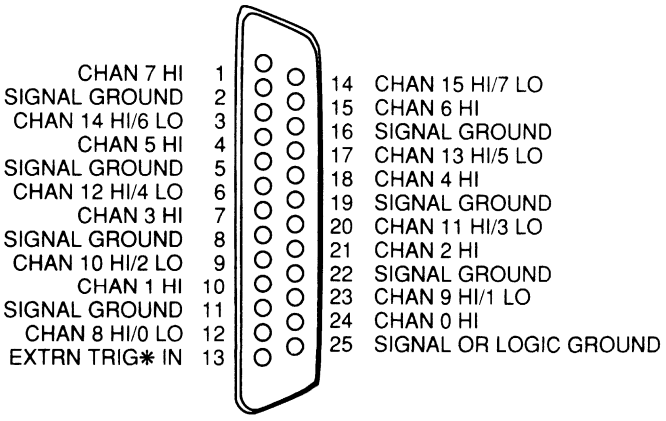


Figure 2. Analog Inputs, P1

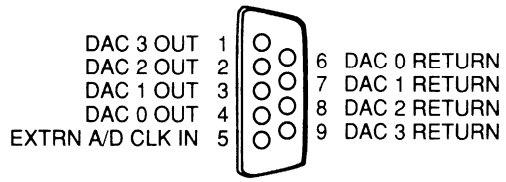


Figure 3. Analog Outputs, P2

ORDERING GUIDE

Model	A/D Bits	A/D Converter Sample Time	D/A Channels
PC-411A	12	12 µSec.	none
PC-411B	14	14 µSec.	none
PC-412A	12	12 µSec.	4
PC-412B	14	14 µSec.	4

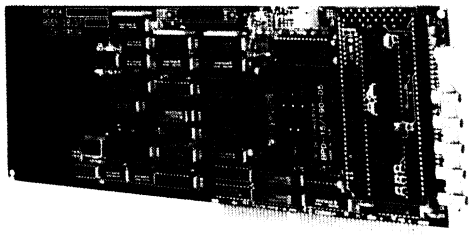
Each board is power-cycled burned-in, tested and calibrated. All models include a user's manual with software examples.

PC-414SET Set up and configuration program. Saves data to disk or memory buffer. Offers calibration and self test. Supplied on MS-DOS 3.5 inch and 5.25 inch disks. Documentation is in the user manual.

PC-DADiSP Signal Display and Analysis worksheet software on 3.5 inch and 5.25 inch MS-DOS disks. Includes manuals and hardware access key.

PC-414
High Speed Analog Input Board for IBM-PC/AT™, PS-30 or EISA Computers

FEATURES



- **Up to 4 MHz sampling**
- **Choice of 12 or 14 bit A/D resolution**
- **Optional 4 Simultaneous Sample/Holds**
- **On-board FIFO memory up to 4096 samples**
- **Very low harmonic distortion**
- **Ideal for FFT's, DSP or array processor "front ends"**
- **Non-bus burst parallel port for seamless recording**
- **Analog input comparator trigger**

DESCRIPTION

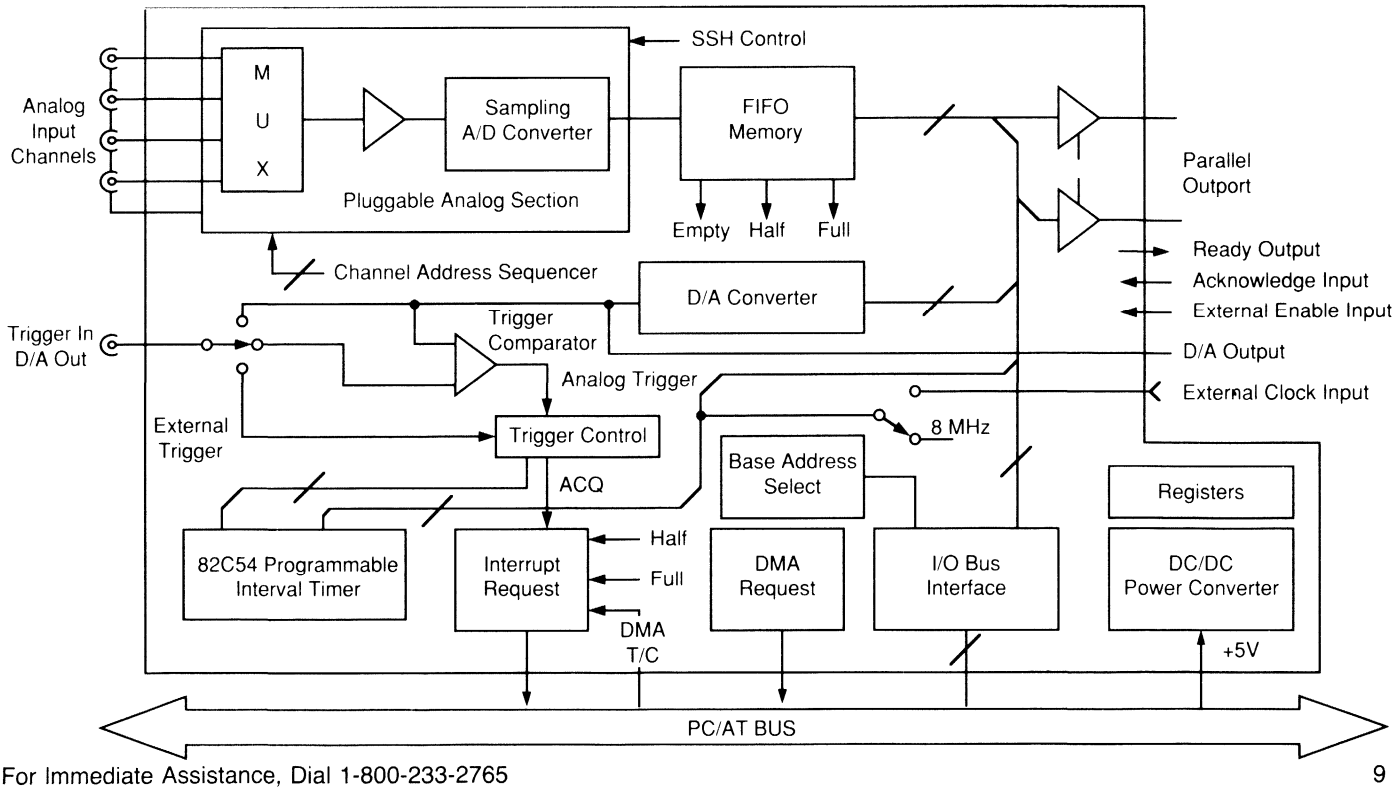
Offering very high system speed, the PC-414 is a multi-channel analog input board for the IBM-PC/AT, PS-30, EISA and compatible computers. Single channel full power input bandwidth is available up to 2.5 MHz and may be sampled at up to 4 MHz. A common motherboard is used, with the analog section contained in a pluggable 2" by 4" module. This allows for a family of several different Sample/Hold - A/D Converter speed and resolution options by exchanging analog modules.

The single-ended analog input ranges of the A/D converter are selectable as unipolar 0 to +10 volts, or bipolar ±5 volts, or ±10 volts depending on model. The gain on the PC-414A may be user-selected times one or times ten for two channels. This offers one-Volt input ranges for receiver signal measurement. Input impedance is 10 megohms to avoid data errors by excessive input signal loading. The input configuration is excellent for analyzing wide band communications signals. Model PC-414E offers 16 single-ended or 8 differential high speed channels.

Model PC-414A uses a Simultaneous Sample/Hold section (SSH). The SSH acquires signals on parallel channels at the same time then the A/D converter rapidly digitizes each held signal sequentially. This provides phase correction and de-skewing of multichannel correlated signals. Applications include high speed cross-channel computation, beam-former coherency for sonar or acoustics, telemetry, multiple carrier demodulation, and highly concurrent system testing.

A/D data passes to an on-board First-In, First-Out (FIFO) data memory and then to the host computer bus interface under software control. The FIFO acts to decouple the precise timing of the A/D section with the block-oriented data transfers on the bus. The design can continuously collect analog data with non-stop converter triggering while data is simultaneously read from the FIFO. This allows the collection of "seamless" wide-bandwidth signals of millions of samples or greater. Functions such as FFT sampling cannot tolerate lost samples without increases in "arithmetic" noise during computation processing.

Data may be transferred to mass storage peripherals such as disk or magnetic tape. Applications include long-baseline studies in astrophysics, component life testing and anomalous pattern search.



The FIFO data output may also be routed under host software control to an on-board parallel data port instead of being sent to the computer bus. This parallel burst channel data may be read by an external processor at very high speeds and avoids possible speed restrictions of the computer bus. The outport uses a very simple ready/acknowledge transfer handshake which is adaptable to any remote parallel port. Possible applications are array processors and mainframe I/O ports.

The analog section of the PC-414 is optimized for high signal quality and very low dynamic noise. The board is designed and qualified with low Total Harmonic Distortion (THD) characteristics. The PC-414 is ideal as an FFT "front end" or DSP quantizer.

The A/D conversion timing section is designed for accurate multi-scan data acquisition. Software programmable timers control the interval between each conversion and each multichannel scan. A programmable sample counter will allow sample blocks of specified length independent of FIFO length. The timer/counter section uses a precision on-board crystal clock and may be replaced by an external timebase. Timeout and sample count activities may be monitored from the computer bus using I/O status registers and/or programmable interrupts. The interrupt method may be fully synchronized with software programmable DMA transfers directly to host computer memory.

S/H-A/D triggering may use several sources under software control. The internal timebase is the normal trigger source although single conversions or scans may be directly commanded by host I/O register writes. An external trigger clock may also be used to precisely synchronize sampling with external events. This external trigger may start a single sample, a single multichannel scan or "N" multiple scans separated by programmable delays.

Analog sampling may also be level-triggered using an on-board analog comparator and an external level input. The reference trigger level to the comparator is derived from an on-board 12-bit D/A converter. If preferred, the D/A converter may also be used as an analog output channel for any purpose.

The PC-414 A thru D contains five signal connectors. Four connectors are for the sampled analog channels. The fifth connector is for a choice of the external timebase clock input, the external analog trigger reference level or for the D/A output. The PC-414E accepts 16S/8D input channels plus trigger.

The computer interface for control and status uses 16-bit I/O addressing. A/D data uses 16-bit transfers under program or host DMA control. A single interrupt is generated for a variety of conditions. These include A/D data ready, DMA terminal count, sample count reached, FIFO half-full or FIFO full.

A/D output data coding is right-justified two's complement with sign extension. This format is excellent for integer data typing with high level computer languages such as "C", FORTRAN, Pascal or Ada. It is also directly compatible with very fast arithmetic instructions for all microprocessor assembly languages and math coprocessors. Straight binary coding may also be selected.

A high-efficiency, low noise DC/DC converter provides quiet power to linear sections. PC-414A-D analog inputs use rear SMA coaxial threaded connectors (DB-25 for 414E). The burst channel parallel output port uses an internal header connector.

Software

A menu-driven windowed setup and configuration program is optionally available on both 5.25" or 3.5" MS-DOS disks. The program automatically adapts to the display type and 80286 or 80386 CPU plus mouse. The program sets the I/O base address, interrupt and DMA systems, loads registers and D/A converter data, starts timers and saves data to disk or memory. The entire hardware configuration may be saved to disk. The software also includes A/D-D/A calibration procedures.

A/D data memory saves may be sent to conventional memory (below 640K) or extended memory (above 1Mb), either by DMA or program transfer. Memory saves may also use XMS memories. Disk data formats include binary integer, IEEE-754 binary floating point and ASCII floating point (Lotus PRN format). The setup program is also available in source language format and includes fast assembly language modules which may be linked to user-written programs.

Users have three methods of implementing PC-414 software; the optional setup/configuration program, third party software or user-written code. Third party display and processing software offers graphic outputs, DSP functions such as FFT's and statistical analysis of data files. Third party packages will accept data by file transfer or fast internal buffer transfer. The buffer method offers a fully integrated package which controls the PC-414 and will display continuous graphic data. Very high speed "streaming mode" file saves are also offered.

For users with a custom applicaton, the user manual has detailed register and timing information for programmers to write their own software in any langauge.

Simultaneous Sample/Hold

In Figure 2, four input signals are sampled at the same time using the PC-414A's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired, they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors from conventional sequential multiplexer scanning.

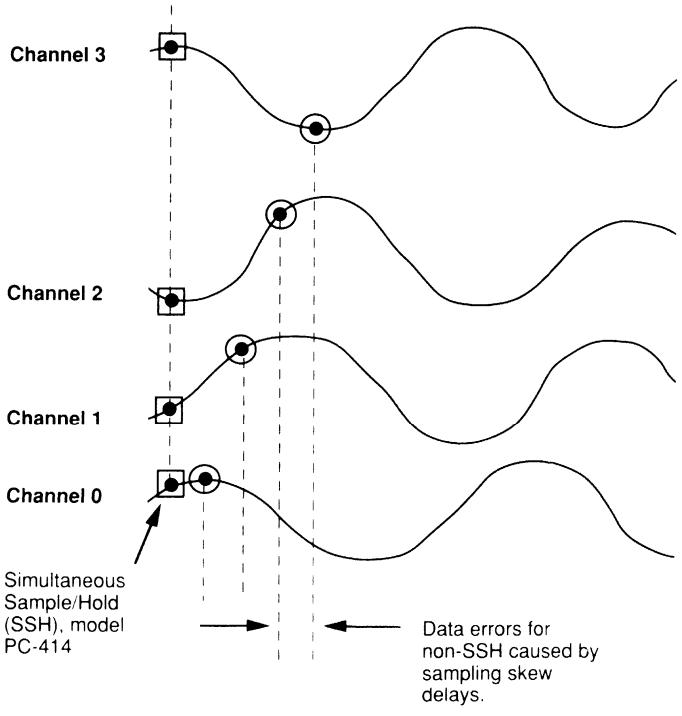


Figure 2. PC-414 Simultaneous Sample/Hold

FUNCTIONAL SPECIFICATIONS (Typical at +25 °C, dynamic conditions, gain=1, unless noted)

ANALOG INPUTS

Number of Channels	4 channels (414A,B,C) 1 channel (414D) 16S/8D channels (414E)			
Input Configuration (non-isolated)	Single-ended (430A,B,C) SE or Differential (430E)			
Full Scale Input Ranges		0 to 10V ±10V	±5V	±1.25V
(user-selectable) [gain = 1]	414A	✔	-	-
	414B	✔	✔	-
	414C	✔	✔	-
	414D	-	-	✔
	414E	✔	✔	-
Programmable Gains	See footnote			
Input Impedance [Note 5]	10 Megohm, min. power on 1.5 Kilohms power off			
Input Bias Current	± 1 nA			
Input Capacitance	10 pF per channel			
Input Overvoltage	± 15 V (no damage)			
O.V. Recovery Time	2 microseconds max.			
Common Mode Voltage Range	±10V max. (414E)			
Common Mode Rejection (DC - 60 Hz)	-80 dB (g=100) (414E)			
Addressing Modes	1. Single channel 2. Simultaneous Sample/Hold 3. Sequential with autosequenced addressing 4. Random addressing by host software			

SAMPLE/HOLD

Acquisition Time (FSR step) to 0.01% of FSR	750 nS max. (414A,E,B) 200 nS max. (414C) 50 nS max. (414D)
Aperture Delay	6 nS (414A) 30 nS (414B,C,E) 10 nS (414D)
Aperture Delay Uncertainty	±1 nS (414A) ±5 nS (414B,C,E) ±10 pS (414D)
Droop Rate	1 µV/µS
SSH Channel-to-channel Linearity Tracking	± 0.03% (414A only)

A/D CONVERTER

Resolution	12 bits (414A,C,D,E) 14 bits (414B)
Conversion Period	500 nanoseconds (414A) 1 microsecond (414B,C,E) 200 nanoseconds (414D)
Output Coding	Positive-true right-justified straight binary (unipolar) or right-justified two's complement (bipolar) with sign extension through bit 15.
Trigger Sources (Software selectable)	1. Local Pacer sample clock 2. External TTL sample clock 3. Analog threshold comp.

TOTAL SYSTEM DC CHARACTERISTICS [See Tech. Note 6]

Integral Non-linearity	±1 LSB of FSR (414A,C,E) ±1.5 LSB of FSR (414B,D)
Differential Non-linearity	± 0.75 LSB of FSR (414A,C,E) ± 1 LSB of FSR (414B,D)
Full Scale Temperature Coefficient	±0.1 LSB per °C (414A,C,D,E) ±0.3 LSB per °C (414B,D)
Zero or Offset Temperature Coefficient	±0.1 LSB per °C (414A,C,E) ±0.3 LSB per °C (414B,D)
Power Supply Rejection	±0.004% per % of bus +5V

A/D MEMORY

Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024 A/D samples, standard. Up to 4096 A/D samples (optional).

TOTAL SYSTEM DYNAMIC PERFORMANCE [Note 1]

System Bandwidth (single channel, FSR input)	1 MHz (414A,C) 200 KHz (414B,E) 2.5 MHz (414D)
Total Throughput to FIFO (single channel, gain=1)	700 nanoseconds (414A) 2 microseconds (414B,E) 1 microsecond (414C) 250 nS (414D)
Throughput to FIFO per A/D sample (sequential channels, gain = 1) [See Tech. Note 3]	1 microsecond (414A) 3 microseconds (414B) 2 microseconds (414C) 4 microseconds (414E)
Throughput to FIFO (sequential channels, gain = 10)	10 microseconds (414A)
Total Harmonic Distortion FS input [See Tech. Note 2]	-72 dB (414A,C,E) -75 dB (414B) -68 dB (414D)

TRIGGER CONTROL

Programmable Interval Timer Type	82C54
Functions	1. A/D sample count reached 2. A/D start rate (16 bit divisor) 3. Scan trigger rate (16 bit divisor)
Pacer Sample Counter	1 to 65,536 samples. Drives the Acquire flag/interrupt gate for A/D start pulses.
82C54 Clock Source	1. Internal 8 MHz crystal clock 2. External TTL input, 10 MHz max.
Scan Trigger Clock	125, 250 or 500 KHz
Analog Trigger Input Range [Note 4]	± 10 Volts (not avail. 414D)
Analog Trigger Response	2 microseconds to set status flag
Analog Trigger Hysteresis	40 millivolts

Footnote:

Resistor-programmed gain from X1 to X100 is available on PC-414E with increased settling delay at higher gain. Fixed gains of X1 and X10 on 2 channels, offering 1V ranges, are selectable on the PC-414A.

ANALOG OUTPUT (not available PC-414D)	
Number of Channels	One Channel
Function (user-selectable)	1. General purpose analog output 2. Threshold comparator for A/D trigger.
Resolution	12 bits
Output Voltage Range (User-selectable)	0 to +10V, ± 5V and ±10V at 5 mA max.
Linearity	± 0.05% of FSR
Settling time (10V step)	5 microseconds to 0.05%
Input Coding	Same as A/D section

PC/AT-BUS INTERFACE	
Architecture	I/O mapped, pluggable to IBM-PC/AT, PS-30, EISA bus and compatibles. Decodes eight 16-bit I/O registers.
I/O Mapping	Decodes I/O address lines A9-A0.
Data Transfer	I/O transfer or host DMA, software selectable.
Data Bus	16 bits.
Direct Memory Access	1 channel, selectable on channels 5, 6 or 7, set by software.
DMA Request Conditions (software selectable)	FIFO full, half full, not empty, scan acquire flag (sample count reached).
Control/Status Functions	Board reset, FIFO flags, interrupt select and status, DMA select and status, trigger source, timer control and period, sample count load, parallel outport enable, A/D enable, MUX auto-sequence.
Number of Interrupts	1 interrupt, selectable on level 7, 9 thru 12, or 15. The interrupt level is set by software.
Bus Interrupt Sources	Scan acquire flag (sample count), FIFO full or half full, DMA terminal count from bus.

PARALLEL PORT	
Parallel Outport	16 data lines, TTL levels from FIFO. Includes ready out, acknowledge in, external clock, and transfer enable in handshakes. Outport steering is software enabled.
Function	Asynchronous slave to external master. Does not provide addressing. The transfer enable input is displayed as a status bit.
Parallel Port Loading	24 mA out, 1.6 mA in
Parallel Port Connector	2-row 26-pin header type mounted on board interior. 0.100" pin spacing suitable for flat cable.
Parallel Port Speed	4 MHz max. data transfer to external processor

MISCELLANEOUS	
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain per channel for SSH on PC-414A. A single offset and gain pot is provided on PC-414B,C,D,E. Recommended recalibration interval is 90 days in stable conditions.
Analog Input Connectors	Four SMA miniature coaxial, mounted on rear slot. Note 7.
Multipurpose Connector (Note 7)	5th SMA user-selectable for: 1. Pacer trigger input 2. Analog threshold comparator input 3. D/A output
Operating Temperature Range	0 to + 60 degrees Celsius
Storage Temp. Range	-25 to +85 degrees Celsius
Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet. Forced cooling is recommended.
Power Required	+5 Vdc @ 3.5 Amps max. from AT bus.
Outline Dimensions	4.5 x 13.31 x 0.625 inches, compatible to PC/AT bus.

Technical Notes:

[1] Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

[2] THD test conditions are:
1. Input freq. 500 KHz (PC-414A) 200 KHz (PC-414B,E)
300 KHz (PC-414C) 1 MHz (PC-414D)

2.Generator/filter THD is -90 dB min.
3.THD computed by FFT to 5th harmonic.

$$THD = 20 * \log10 \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}$$

4. Inputs are 1/2 full scale. No channel advance.
5. A/D trigger rate=1.5 MHz (PC-414A), 500 KHz (PC-414B,C,E), 4 MHz (PC-414D)

[3] The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the PC-414C were scanned, the maximum sample rate on any one channel would be 2 microseconds X 4 channels = 8 microseconds (125 KHz per channel).

[4] For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10 Volts.

[5] The input impedance of 10 Megohms minimum avoids attenuation errors from external input source resistance. For many applications, an in-line coaxial 50-ohm shunt, inserted adjacent to the front connectors, is recommended to reduce reflections and standing wave errors. The 414D input is 50 ohms.

[6] Allow 20 minutes warmup time to rated specifications for model PC-414B.

[7] A 25-pin DB-25S connector is used for the PC-414E.

I/O Register Memory Mapping

The base address may be selected anywhere up to 3F0h on 16-byte boundaries.

I/O Address (hex)	Direction	Description
Base + 0	Write	Command Register
Base + 0	Read	Status Register
Base + 2	Write	Channel Address Register
Base + 4	Write	D/A Data Register
Base + 6	Write	FIFO Reset Register
Base + 6	Read	FIFO A/D Data Register
Base + 8	Read/Write	Counter #0 (82C54)
Base + 0Ah	Read/Write	Counter #1 (82C54)
Base + 0Ch	Read/Write	Counter #2 (82C54)
Base + 0Eh	Read/Write	Control Register (82C54)

At power-up or PC bus reset, all registers contain zeroes except the FIFO HF and FF bits. The registers may be programmed in any sequence as long as the command register is last. Use 16-bit I/O word operations.

Command Register (Write BASE + 0)

15 14	13 12 11	10 9	8 7	6	4	3	2	1	0
DMA Lvl	Intrpt Lvl	DMA Req	Intrpt Req	Prt/ Bus	Trg Pol	Aut Inc	Scn En	Cn En	Trg Src
1 0	2 1 0	1 0	1 0						

Bits not shown or "x" bits are not used or don't care.

Trigger Source [Bit 0]
0 = Sample from the internal trigger
1 = Sample from the external trigger

Internal triggers are generated from the 82C54 timer. Each internal trigger will enable sampling until the sample count is done or command 1 = 0. For continuous triggering, use timer mode 2. For a single trigger, set timer mode 5 and enable the A/D converter.

The external trigger may be from the analog threshold comparator or the digital TTL trigger.

Convert Enable [Bit 1]
0 = Disable A/D conversion (default)
1 = Enable A/D conversion

Scan Enable [Bit 2]
0 = One A/D conversion per A/D start clock
1 = Up to 16 A/D conversions per A/D start clock (set by the channel address register).

Channel Address Auto-increment [Bit 3]
0 = Single channel (no increment)
1 = Sequence channel address at A/D conversion (The address counter will wrap around from channel 15 to 0).

External Trigger Polarity [Bit 4]
0 = Trigger on falling edge (default)
1 = Trigger on rising edge

Bit 5
Not used

Select FIFO Output Data Steering [Bit 6]
0 = Select PC bus data register (Inhibit parallel port)
1 = Enable FIFO transfers to parallel port (Inhibit PC bus data access)

Interrupt Request Source

Bit 8	Bit 7	
0	1	= Interrupt on FIFO full
1	0	= Interrupt on FIFO half full
0	0	= Interrupt on data Acquire flag
1	1	= Interrupt on terminal count of DMA completion (required for DMA).

DMA Request Source

Bit 10	Bit 9	
0	1	= DMA request on FIFO full (block mode)
1	0	= DMA request on FIFO half full (block mode)
0	0	= DMA request on data Acquire flag (block mode)
1	1	= DMA request on FIFO not empty (demand mode)

Block Mode: After setting up the DMA controller registers, a DMA block transfer will occur on a DMA request. At the end of the transfer, the PC-414 will generate a terminal count interrupt.

Demand Mode: This is identical to the Block Mode except that the transfer will continue as long as the FIFO is not empty. The transfer will stop when the FIFO is empty or a terminal count occurred at the end of a 64K word transfer.

Interrupt Level Select

Bit 13	Bit 12	Bit 11	
0	0	0	= Interrupt disable
0	0	1	= Interrupt request on IRQ 7
0	1	0	= Interrupt request on IRQ 9
0	1	1	= Interrupt request on IRQ 10
1	0	0	= Interrupt request on IRQ 11
1	0	1	= Interrupt request on IRQ 12
1	1	0	= Interrupt request on IRQ 15
1	1	1	= Not used

DMA Level Select

Bit 15	Bit 14	
0	0	= DMA disable
0	1	= DMA request on DRQ 5
1	0	= DMA request on DRQ 6
1	1	= DMA request on DRQ 7

Channel Address Register (Write BASE + 2)

15 - 8	7 6 5 4	3 2 1 0
Not Used	Scan Control 3 2 1 0	Channel Address 3 2 1 0

Channel Address [Bits 3 - 0]
Only bits 1 and 0 are used for the 4-channel analog modules. All 4 counter bits are available at the A/D module.

Scan Control [Bits 7 - 4]
In the scan mode (command 2=1), each A/D start convert pulse will cause multiple A/D conversions as selected by these bits. Each scan starts from channel zero.

Status Register (Read BASE + 0)

15 - 8	7	6 5 4	3	2	1	0
Not Used	Xfr In Pro	FIFO Status FF HF EF	Ovr Smp Err	Ana Trg Lvl	EOC Sts	ACQ Sts

Acquisition Status [Bit 0]
0 = A/D scan not in progress or scan done (Counter 0 sample count was reached).
1 = A/D scan in progress (Counter 0 sample count not reached).

End of A/D Conversion Status (EOC) [Bit 1]
0 = A/D conversion in progress, data invalid
1 = A/D conversion done, data valid

Analog Trigger Comparator Output [Bit 2]
0 = Analog trigger input is below reference
1 = Analog trigger input is above reference

Oversample Error [Bit 3]
0 = No error
1 = A/D was triggered before EOC is done.

Bit 3 is cleared by disabling A/D conversions (write command 1=0).

FIFO Status Flags
Bit 4: 0=FIFO is empty, 1= FIFO not empty
Bit 5: 0=FIFO is half full or greater, 1=less than half full
Bit 6: 0=FIFO is full, 1=FIFO is not full

NOTE the negative true coding on these bits.

Transfer in Progress [Bit 7]
0 = Remote receiver is not ready for transfer
1 = Remote receiver is ready for transfer

Bit 7 displays parallel inport pin 2 (external Transfer Enable In) ANDed with command bit 6.

D/A Data Register (Write BASE + 4)

15-12	11	10	9	8	7	6	5	4	3	2	1	0
x-x	DA1 MSB	DA2	DA3	DA3	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12 LSB

FIFO Reset Register (Write BASE + 6)

15	0
x	x

Any write to this register will clear the FIFO and set the empty flag true. If A/D conversion is still running, the FIFO will be not empty when the next A/D sample EOC occurs.

FIFO Data Register (Read BASE + 6)

15	14	13	12	11 00
S	S	S	S	MSB - - LSB 12 ALL

12-bit A/D data

15	14	13 00
S	S	MSB - - - LSB 14 ALL

14-Bit A/D Data

"S" bits are sign-extended from either bit 11 (12 bit A/D's) or bit 13 (14-bit A/D's) in bipolar input range. For unipolar ranges, S = 0.

82C54 Programmable Interval Timer

[Refer to the PC-414 User Manual for detailed programming information]

Counter Register
(Read/Write BASE + 8 - Counter #0)
(Read/Write BASE + 0Ah - Counter #1)
(Read/Write BASE + 0Ch - Counter #2)

15 8	7	6	5	4	3	2	1	0
x - x	C07	C06	C05	C04	C03	C02	C01	C00

Control Word Register (Read/Write BASE + 0Eh)

15 8	7	6	5	4	3	2	1	0
x - x	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Select Counter

SC1	SC0	
0	0	Select counter #0
0	1	Select counter #1
1	0	Select counter #2
1	1	Read back command

Read/Load

RL1	RL0	
0	0	Counter latch operation
0	1	Read/Load LSB only
1	0	Read/Load MSB only
1	1	Read/Load LSB then MSB

Mode

M2	M1	M0	
x	1	0	Rate generator
1	0	0	Software trigger
1	0	1	Hardware trigger

BCD

BCD	
0	16-bit binary count
1	4-decade binary coded decimal count

Transfer Speeds

PC/AT bus transfer rates are host dependent and should be determined by testing. For example, a 33 MHz 80386 Compaq achieved 1.5 megasamples/second instantaneous sample-to-sample timing using the REP INSW instruction. To optimize throughput, disable all possible interrupts. Transfers to hard disk may exceed 150 K samples/second using special techniques.

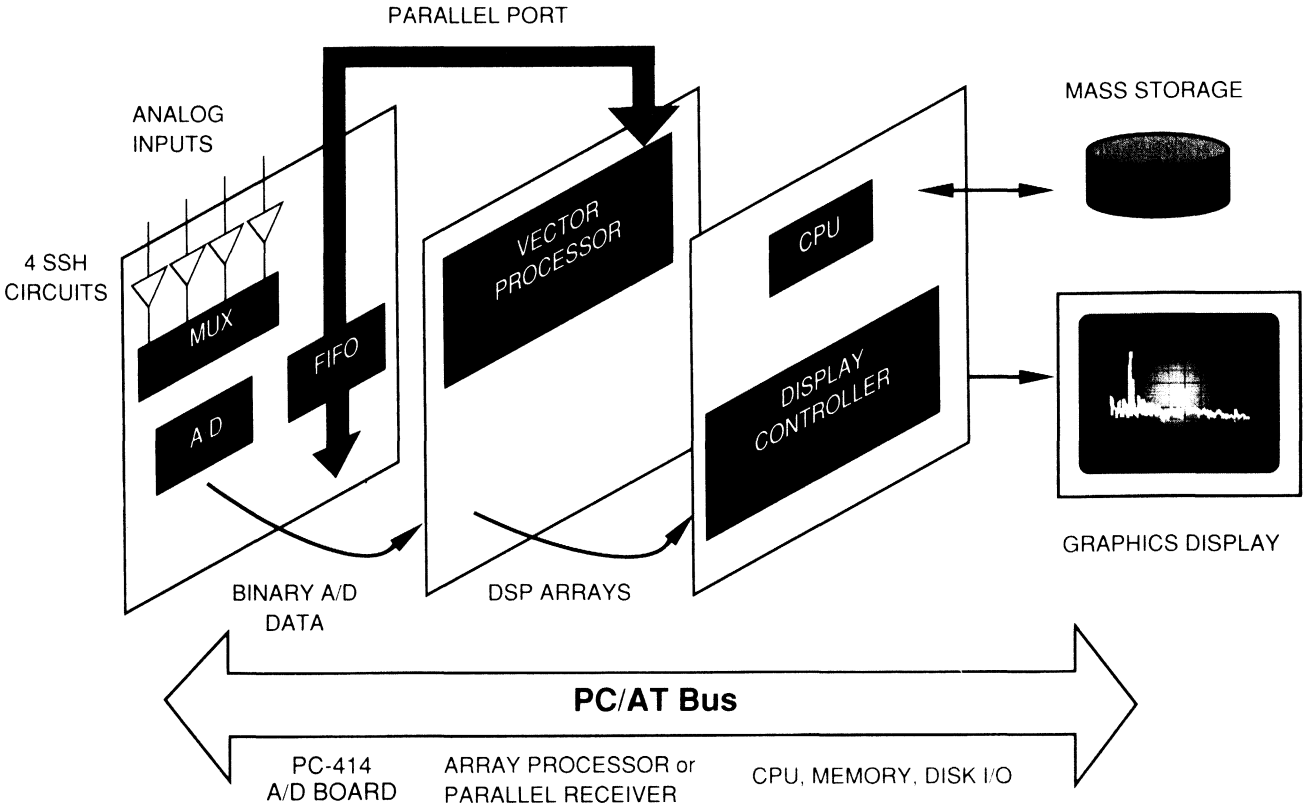


Figure 3. Array Preprocessing

Array Preprocessing

Figure 3 shows the PC-414 installed in a typical PC/AT application. The PC-414 may be connected to an array processor board via a parallel port or the PC/AT bus. The parallel port offers higher speed by offloading block data transfers from the PC/AT bus. A separate cable is required for the parallel port.

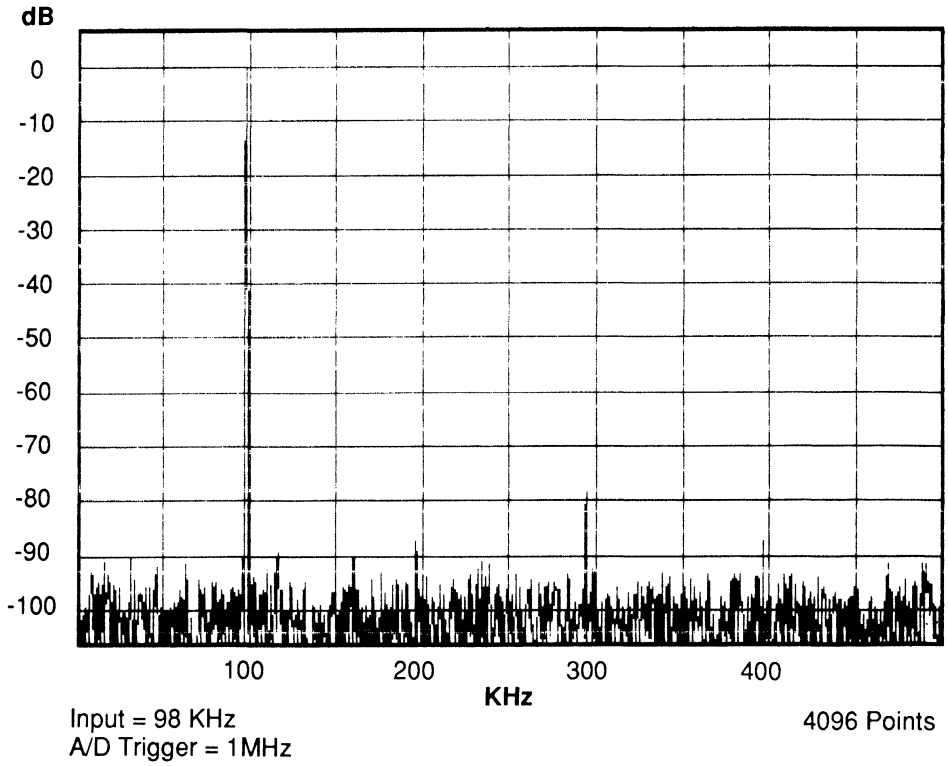


Figure 4. PC-414 FFT Diagram

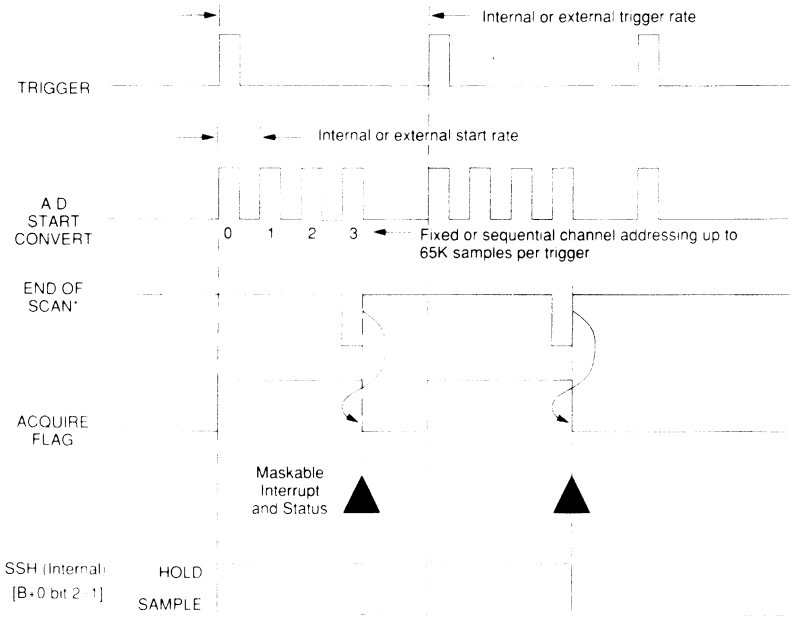


Figure 5. PC-414 Timing Diagram

Ordering Guide

Model	A/D Bits	Chans.	Sample rate single chan.	FIFO A/D samples	Simul.S/H	PGA
PC-414A1	12	4 SE	1.5 MHz	1024	4 chans.	x1,x10
PC-414A2	12	4 SE	1.5 MHz	4096	4 chans.	x1,x10
PC-414B1	14	4 SE	500 KHz	1024	none	none
PC-414B2	14	4 SE	500 KHz	4096	none	none
PC-414C1	12	4 SE	1 MHz	1024	none	none
PC-414C2	12	4 SE	1 MHz	4096	none	none
PC-414D1	12	1 SE	4 MHz	1024	none	none
PC-414D2	12	1 SE	4 MHz	4096	none	none
PC-414E1	12	16S/8D	250 KHz (scan)	1024	none	1-100
PC-414E2	12	16S/8D	250 KHz (scan)	4096	none	1-100

61-7342340 SMA male to BNC male coaxial cable, 1 meter length. (One cable required per channel)

Each board is power-cycle burned-in, tested and calibrated. All models include a user's manual. The warranty period is one year.

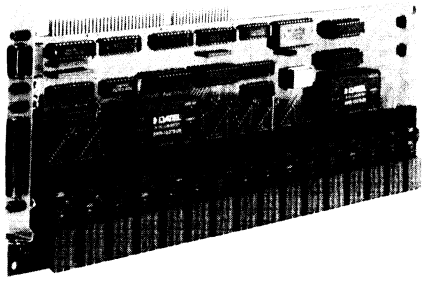
Software:

PC-414SET	Setup/configuration program. Includes executable files on both 3.5-inch 720K and 5.25-inch 1.2M MS-DOS disks.
PC-414SRC	Source code to setup and configuration program on both 3.5-inch and 5.25-inch MS-DOS disks. Includes "C" and assembly source code and window driver library. Documentation is on disk.
PC-DADISP	Signal Display and Analysis worksheet software on 3.5-inch and 5.25-inch disks. Includes manuals.

PC-422
Fast Simultaneous 16-Channel PC/AT Analog Output Board

FEATURES

- **8 or 16 analog outputs**
- **12-bit D/A resolution**
- **3 Microsecond settling time**
- **Simultaneous update**
- **Trigger timer interrupt**
- **Digital I/O (4-In, 4-Out)**
- **Output ranges selectable per channel**



DESCRIPTION

Many applications require phase-synchronous analog outputs. Examples include precision system simulation and coherent field generation in process control, audio, acoustics and sonar. The PC-422 is a high density analog output board with up to 16 signal channels. Each Digital to Analog Converter (DAC) channel may be individually selected for full scale output ranges of 0 to +5V, 0 to +10V, ±5V or ±10V. All outputs are buffered and will deliver ±0.025% accuracy from 0 to 5 milliamps output load. The PC-422 is installed in a host IBM-PC/AT or compatible computer.

To achieve the simultaneous update capability, each channel input register is double buffered. The registers are successively loaded by the host computer then all channels are updated by host command or trigger. If preferred, each channel may also be operated in the non-concurrent transparent mode under program control with random addressing or single channel operation.

For applications requiring a precision clock to sequence the output waveforms, the PC-422 includes a software-programmable trigger. The trigger strobes the simultaneous update and posts a status bit or interrupt to the host PC. Upon detecting the trigger, the host may block-load the next data frame. The trigger may be derived from an internal crystal-stabilized timer or from an external timer base. The external trigger option makes the PC-422 fully synchronous with external events. The trigger section includes a spare output counter, usable for any purpose.

For repeating frame scan applications, the PC-422 includes an auto-increment mode. In this mode, block transfer I/O string instructions will automatically load up to 16 channels at very high speed from a memory buffer in the PC. The PC-422 will digitally steer each analog data word to successive DAC input registers while using the same I/O data register address. The user's program simply maintains the 80X86 CX register as a downcounter to terminate each block transfer. Typically, the trigger and auto-increment modes are used together where the PC loads the next block after detecting the trigger status signal from the last simultaneous update.

The combination of a precision frame clock trigger, auto-increment channel addressing and high speed simultaneous block loading make the PC-422 ideal for artificial waveform applications. Such waveform generators continuously loop through a large RAM buffer containing a synthetic composite digitized analog signal.

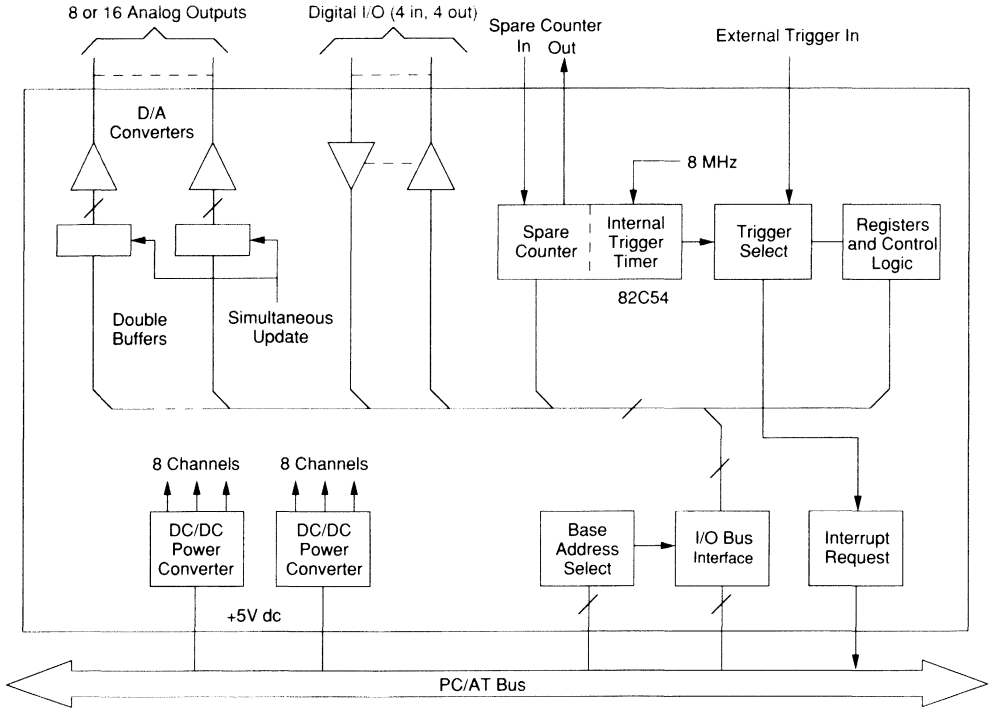


Figure 1. PC-422 Block Diagram

GENERAL DESCRIPTION CONT.

Fast settling rates are another feature of the PC-422. Full scale step response of each DAC channel is 3 microseconds. Block transfers of input data may occur faster than individual DAC channel analog settling times. Each DAC channel input register can be updated at over 1 Megasample per second.

The PC-422 is configured on a PC/AT compatible board measuring 4.5 inches high by 13.31 inches long. Analog signal connections are made using a rear panel 25-pin "D" connector. Eight digital channels (4 inputs and 4 outputs) of discrete I/O are provided for general purpose control and monitoring of external logic devices. A 9-pin "D" connector provides digital I/O. The PC-422 includes two high efficiency DC to DC power converters to supply local analog circuits. The entire board uses only +5 Volt DC power from the PC/AT bus. The board is compatible with all popular computer languages although the highest speed will require assembly language. A comprehensive user's manual is included with the board showing full programming and application information.

SPECIFICATIONS

(typical at +25 °C, dynamic conditions, unless noted)

ANALOG OUTPUTS	
Number of Channels	8 or 16
Output Configuration	single-ended, non-isolated
Full Scale Output Ranges	0 to +5V, 0 to +10V, ±5V, ±10V, individually selectable per channel.
Output Current	0 to ±5 mA min. (source or sink), short-circuit protected to ground.
Resolution	12 binary bits.
Input Data Coding	Straight or offset binary, positive true coding. Data is right justified. See note 3.
Output Impedance	50 milliohms
Channel Addressing Modes	Random, simultaneous or auto-increment sequential.

PERFORMANCE	
Monotonicity	No missing codes
Linearity Error (after calibration)	±0.025% of FSR
Temperature Coefficient of Gain	±5 ppm typ.,±30 ppm max. of FSR/ °C max.
Temperature Coefficient of Zero or Offset	±20 ppm of FSR/ °C max.
Settling Time (FS step)	3 µsec max. to ±0.025% of final value. (0-5V,0-10V, ±5V ranges). 4 µsec max. for ±10V range.
Settling Time (1 LSB step)	1 µsec to ±0.01%
Slew Rate	10 V/µSec min.

DIGITAL INPUT/OUTPUT	
Number of Lines	4 inputs, 4 outputs, non-isolated
Logic Levels	Compatible with TTL, TTL-LS, ALS, etc. Inputs: "0"<0.8V, "1">2.0V Outputs: "0"<0.4V, "1">2.4V
I/O Loading	Inputs: 1 LS load plus 10 KΩ pullup to +5V. Outputs: 24 mA source or sink

COUNTER/TIMER	
Function	Used as an update strobe for each multichannel DAC frame.
Frequency Range	2 MHz to 536.87 seconds (32-stage binary or BCD divider).
Frequency Stability	± 50 ppm/ °C
Spare Counter	16-stage binary divider usable for any purpose. Will divide input signals from 2 to 65,535. Includes counter input and output, 1 TTL-LS load, 10 MHz max input.

PC/AT BUS INTERFACE	
Architecture	I/O mapped in 8 contiguous word locations on 16-byte boundaries.
I/O Mapping	Decodes I/O address lines A9 through A4. Maximum base address is 3F0h.
Data Bus	16-bit I/O transfer.
Trigger Interrupt	1 interrupt, software-selectable on level 7, 9, 10, 11 or 15.

MISCELLANEOUS	
Analog Section Adjustments	Full scale gain and zero or offset potentiometers are provided for each DAC channel. See note 2.
Analog Connector [P1]	25-pin DB-25S, also includes the external trigger input.
Digital I/O Connector [P2]	9-pin DB-9S
Spare Timer/Counter	On-board header pins
Operating Temp Range	0 to +60 °C
Storage Temp Range	-25 to +85 °C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet (0-3048 m). Forced cooling is recommended.
Power Supply Requirements	+5 V dc, ± 5% supplied from PC/AT bus. 2.5 Amps typ., 4.0 Amps max. (16 channels), 1.5 Amps typ., 2.5 Amps max. (8 channels).
Outline Dimensions	4.5" H. x 13.31" L x 0.5" W (11,43 x 33,81 x 1,27 cm)
Weight	1.5 pounds (0,7 Kg)

Notes

1. Depending on the host PC type, I/O transfers may occur over 1 megasample per second. For example, using the REP OUTSW instruction, a Compaq 33 MHz 80386 host achieved approximately 630 nanoseconds instantaneous sample to sample timing. When estimating system timing, account for any remaining interrupts required (such as the real time clock) and DRAM refresh delays, if any.

2. Recalibration is recommended at 90 day intervals, depending on conditions.

3. All DAC input registers reset to zero or half-scale (0800h) at power-up or bus reset, depending on the unipolar/bipolar switch selection.

PROGRAMMING NOTES

There are three ways to cause an update of the DAC registers. Either a register write may be used, or the internal trigger clock or an external digital trigger input.

To load multiple scans from a large host memory array, use the following sequence:

Program the channel address register for the starting address. Program the command register for auto-increment and trigger updating. Load the first scan into the data channels. Your load program will have to count the number of loads then exit.

1. Poll the status register to detect the trigger. If the trigger was not received, continue polling.

2. When the trigger occurs, optionally test the overrun flag and report any errors. To save time, overrun testing may be deleted if you are sure no data was lost.

3. When the trigger occurs, block load the next data scan while advancing the PC's buffer memory address pointer. For the highest speed, use the 80X86 CX register or other index as a downcounter to terminate the load. Also, if this is a circular host buffer, remember to wrap the pointer to the bottom of the buffer when it reaches the top.

4. If the DAC channel address did not wrap around exactly to channel zero, write the new start channel address.

5. Write to the simultaneous update register to arm the trigger update ready flag.

6. If more scans are needed, go to step 1.

Trigger status polling should be used for the very highest speed. If somewhat lower update rates are needed, DAC refresh may use either the trigger interrupt or by polling. The trigger interrupt is especially useful if other system tasks are concurrent, such as disk I/O or graphics screen writes.

I/O REGISTER MAPPING

The base address may be selected anywhere up to 3F0h on 16-byte boundaries. At power-up or PC bus reset, all control registers contain zeroes. The DAC data register should be programmed after setting up the channel address and command mode. The 82C54 registers must be programmed in a specific sequence, discussed in the user manual. 16-bit I/O word instructions must be used. Unlisted registers are not used.

I/O Address (hex)	Direction	Description
BASE + 0	Write	Command Register
BASE + 0	Read	Status Register
BASE + 2	Write	DAC Channel Address Register
BASE + 4	Write	DAC Data Register
BASE + 6	Write	Simultaneous Update Register
BASE + 8	Read/Write	Counter 0 (82C54)
BASE + 0Ah	Read/Write	Counter 1 (82C54)
BASE + 0Ch	Read/Write	Counter 2 (82C54)
BASE + 0Eh	Read/Write	Control Word Register (82C54)

Note: "x" bits are "don't care".

COMMAND REGISTER (Write I/O BASE + 0)

15 - 11	10 9 8	7	6	5	4	3 2 1 0
Not Used	Intrpt Level 2 1 0	Simul Updt Sel	Simul Updt Mode	Ext/ Int Trig	Chan Auto Incr	Digital Outport 3 2 1 0

Digital Outport [Bits 3, 2, 1, 0] — Discrete digital outputs are written to these bits.

Channel Address Auto-increment [Bit 4]
0 = No channel increment
1 = Increment channel address after a DAC data register write.

In the non-increment mode (bit 4 = 0), successive writes to the DAC data register will load into a single DAC channel selected by the last address written into the channel address register.

In auto-increment mode (bit 4 = 1), the channel address will advance after each data register write. The address will cycle around to channel 0 after reaching channel 15, modulo 16.

Trigger Source Select [Bit 5]
0 = Internal trigger
1 = External trigger

The trigger may be supplied either from the internal clock (counters 0 and 1) or from an external digital trigger input. In the update mode (bit 6 = 1, bit 7 = 1), the trigger strobes all DAC channels simultaneously from previously written DAC data.

Simultaneous Update Mode [Bit 6]
0 = Update via the simultaneous update register (Write BASE + 6).
1 = Update via internal or external trigger.

Simultaneous update causes all 8 or 16 DAC channels to be loaded with data that was last written to their input registers. If command bit 6 = 0, the trigger will be inhibited.

Simultaneous Update Select [Bit 7]
0 = Transparent mode (immediate DAC conversion of input data)
1 = Hold data until update.

With bit 7 = 0, DAC analog outputs will follow their input data values as fast as those values are written. If bit 7 = 1, updating the DAC outputs will wait until the trigger or a write to the update register.

Interrupt Level Select — Bit 10 9 8

10	9	8	
0	0	0	= No interrupt
0	0	1	= Interrupt Request Level 7
0	1	0	= Interrupt Request Level 9
0	1	1	= Interrupt Request Level 10
1	0	0	= Interrupt Request Level 11
1	0	1	= Interrupt Request Level 15
1	1	0	= No interrupt
1	1	1	= No interrupt

These bits select the IRQ line on the PC/AT bus where trigger interrupts are placed.

STATUS REGISTER (Read I/O BASE + 0)

15	14	13 12	11 - 8
Update Ready Status	Over Run Error	Not Used x x	Current Channel Address 3 2 1 0

7	6	5	4	3 2 1 0
Simul. Update Select	Simul. Update Mode	External/ Internal Trigger	ChanAddrs Auto Increment	Digital Inport 3 2 1 0

Bits 4-11 may be used to verify bits loaded into the command register.

Digital Inport [Bits 3, 2, 1, 0] — Discrete digital inputs may be read in these bits.

Status Bits [Bits 7-4] — These bits follow the corresponding bits in the command register.

Current Channel Address [Bits 11-8] — These bits indicate either the last address written into the channel address register or the next channel address to be written to by the next DAC data write.

These addresses will sequence from channel 0 to 15, modulo 16 in auto-increment mode.

Overrun Error [Bit 14] — In trigger update mode (command 6 = 1) this bit will be set to one if a trigger occurs before the next load of the DAC data register. Any write to the command register resets bit 14 to zero.

Update Ready Status [Bit 15] — With command bit 7 = 1, a write to the simultaneous update register will set bit 15 to one. The trigger will reset this bit to 0, indicating that the next frame of data may be loaded. If a trigger occurs before bit 15 is set to 1, the overrun error bit will be set to 1.

Bit 15 is normally polled to detect the trigger after loading the data registers. Bit 15 stays at 0 if command bit 6 = 0.

ORDERING GUIDE

Model	Number of channels
PC-422A	8
PC-422B	16

Boards are fully tested and include a manual.

PC-422SET Setup and configuration program on 3.5-inch and 5.25-inch MS-DOS disks. Provides calibration and test waveforms.

CHANNEL ADDRESS REGISTER (Write I/O BASE + 2)

15 - 4	3 2 1 0
Not Used	Channel Address 3 2 1 0

In non-auto-increment mode, these bits select the address of the next channel to be written to by the DAC data register. The address must be selected before writing data to a channel.

In auto-increment mode, these bits determine the starting channel address. After each data register load, addressing is automatically sequenced. The addressing cycles around to channel 0 after reaching channel 15.

If exactly 16 samples are loaded and the address sequences around to channel 0, this address register will never need reloading after each scan.

DAC DATA REGISTER (Write I/O BASE + 4)

15 - 12	11	---	0
Not Used	DAC MSB		DAC LSB

12-bit DAC data are right justified with the most significant bit at bit 11. In bipolar coding, bit 11 indicates polarity (0 = negative, 1 = positive).

SIMULTANEOUS UPDATE REGISTER (Write I/O BASE + 6)

15 - 8	7 - 0
Not Used	x - x

This register has two separate functions. If command bit 6 = 0 and command bit 7 = 1, the analog outputs of all DAC channels will be updated at the same time by writing any value to this register.

If command bit 6 = 1, writing any value to this register will set the trigger ready status flag (status bit 15) to 1. The flag will remain set until cleared to zero by the trigger. This sequence provides a ready/acknowledge handshake to load data frames without losing samples.

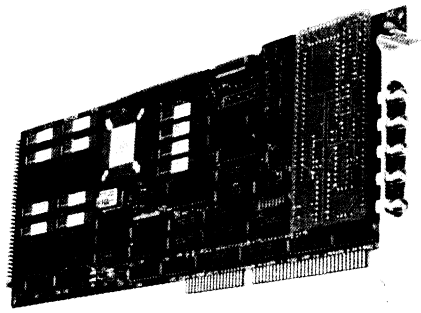
CODING TABLE

Input Code (hex)	Output (unipolar)	Output (bipolar)
0FFFh	+Full scale -1 LSB	+Full scale -1 LSB
0801h	1/2 FS +1 LSB	+1 LSB
0800h	1/2 full scale	Zero
07FFh	1/2 FS -1 LSB	-1 LSB
0000h	Zero	-full scale

PC-430
Very High Speed A/D-DSP Coprocessor Board for IBM-PC/AT

FEATURES

- **Up to 4 MHz A/D sample rate**
- **Choice of 12 or 14-bit A/D resolution**
- **4-Channel Simultaneous Sample/Hold's are optional**
- **On-board 320C30 32 MHz digital signal processor**
- **512 kilobytes dual-ported RAM**
- **Two 1K x 32 internal DSP RAM**
- **8K x 32 expansion RAM**
- **On-board DSP Library - FFT's, filters, matrix math, floating point, etc.**
- **Fast, simple, powerful command executive and driver. No local programming required.**
- **DMA and Interrupt to PC/AT host**
- **Operates with: IBM-PC/AT™ PS-30, EISA computers and compatibles**



GENERAL DESCRIPTION

Advanced performance from the PC-430's on-board Digital Signal Processor (DSP) offers a broad range of high speed waveform analysis and recording applications. The PC-430 will acquire up to sixteen analog input channels, digitize them and store them in local memory while DSP math processing and data transfer is done concurrently. The system is intended for preprocessing "seamless" A/D data streams to mass storage.

The PC-430 is ideal for non-stop, continuous Fast Fourier Transform (FFT) processing, communications receiver signal collection to disk or simultaneous graphics display of spectral data. Application areas include signal recovery from noisy channels, harmonic distortion analyzers and vibration/resonance filtering systems. For use with ultrasonic, sonar or acoustic signals, the interrupt-driven, simultaneous block transfers of data insure no information loss. Other uses include high speed mapping and imaging, satellite channels, astrophysics, seismology, biomedical signals, array processing, control systems, simulators, engine analyzers, aerodynamics, and vehicle systems.

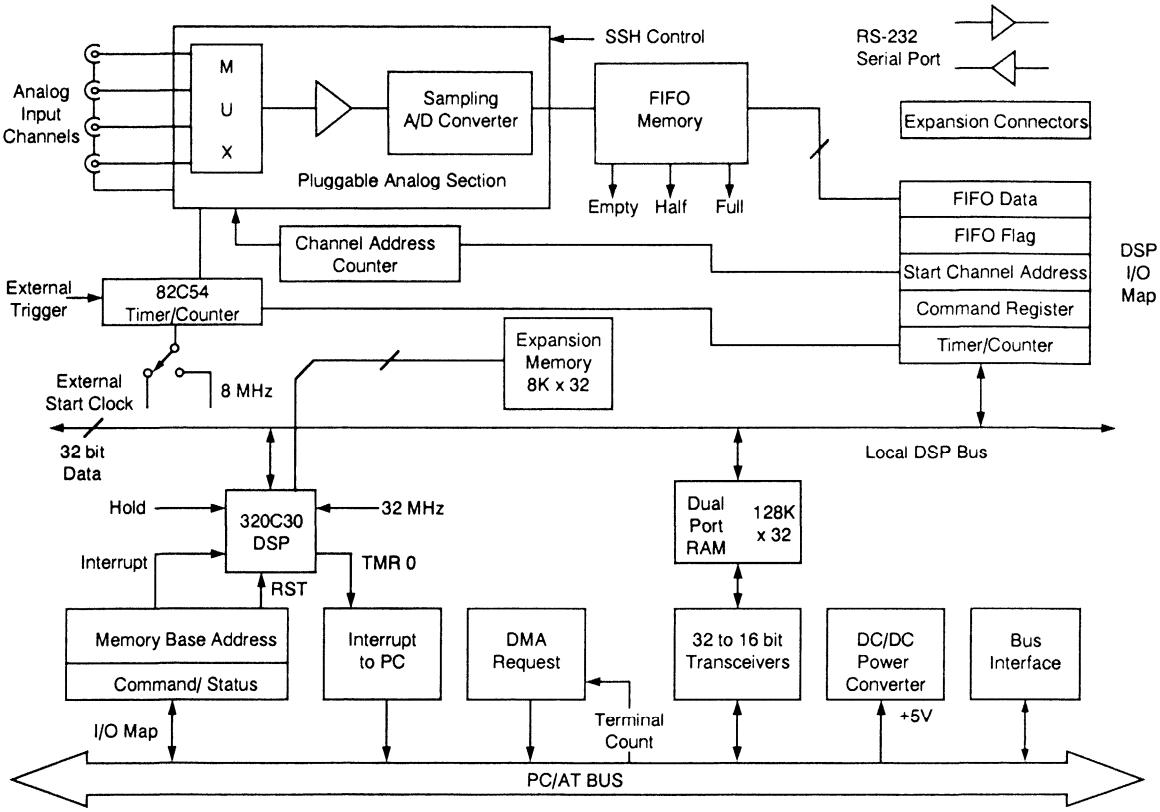


Figure 1. PC-430 Simplified Block Diagram

The board consists of a pluggable analog input subsection, timer-counters, DSP central processing unit (CPU), dual port RAM, local RAM, bus interface, registers and DC power supply. Input signals pass through a very high speed channel multiplexer (except Model PC-430D) to a sampling analog-to-digital (A/D) converter. On Model PC-430A, all four channels are acquired simultaneously by a quad simultaneous sample/hold (SSH) section. A choice of speeds and resolution is offered in the analog section.

A/D triggering for spectral and FFT applications must be precisely controlled. This is handled by a programmable timer-counter section which can control the interval between A/D conversions and the interval between multi-sample A/D scans. The number of samples may also be counted for repeating array sampling. The timer-counter may use an on-board crystal oscillator or an external timebase for precision phase-tracking. The digital output of the A/D passes directly to a first-in, first-out (FIFO) memory. The FIFO acts to decouple the precision timing of the A/D section with the block transfers governed by the DSP internal direct memory access (DMA) controller. Additional timers internal to the DSP are also used.

A/D FIFO data may be sent to dual port random access memory (DPR) shared with the host PC/AT bus. The DPR is organized as 128K by 32 bits. Block transfers may be controlled by the DMA controller in the DSP. The DMA may run in background while math processing continues. Local FIFO and DMA interrupts to the DSP arbitrate these activities. Typically, a swapped dual buffer method is used so that samples are not lost during other processing. Local hardware registers control all A/D, FIFO, and trigger activity.

Single cycle fetch and execution, zero-overhead of looping instructions, software variable wait states, block repeat and an internal instruction cache memory are some of the advanced high speed features of the Texas Instruments 320C30 DSP. The DSP uses 32-bit local data paths for very high speed. Data passed to the host PC/AT bus uses 32-to-16 bit transceivers to the DPR. Simultaneous access attempts to the DPR by both the PC/AT host and the DSP are resolved by high speed arbitration logic. The DSP also has a separate 8K by 32-bit local expansion memory for the stack or temporary data. The architecture of the DSP allows simultaneous processing of two tables from two sections of memory. This provides optimum processing of FFT's and other array functions.

The PC-430 appears as both I/O and memory addresses to the host PC/AT. The I/O base address is selected by on-board switches whereas the memory base address is software programmed through the I/O registers. At power up, the PC-430 appears disconnected from host memory and must be enabled through the I/O registers after writing the memory base address. Since the DPR occupies 512 kilobytes, it will be located in extended memory at 10 0000h or above for most PC's. The PC-430 will operate with 80286, 80386, and 80486 CPU's. The DPR may be addressed up to 16 megabytes.

Access to extended memory is provided in the Executive software package. After loading in the Executive from disk to the DPR, the DSP is transitioned from reset to run using an I/O control bit. The board may be reset at any time or relocated to another memory base address using this technique. The comprehensive Executive Software Package offers fast A/D sample collection and DSP math without writing any local programs. A simple, powerful, high speed command list is used to access the local DSP library. The Exec controls very fast buffer transfers to disk or memory using PC bus interrupts generated from the PC-430. Either host DMA or program transfers may be used. Host DMA and interrupt levels are also software programmed from the I/O registers.

Datel recommends installing the PC-430 in a high quality name-brand host computer. Integrity of bus loading and timing is especially important with high speed boards such as the PC-430.

Simultaneous Sample/Hold

As shown in Figure 2, four input signals are sampled at the same time using the PC-430's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired, they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors from conventional mux scanning.

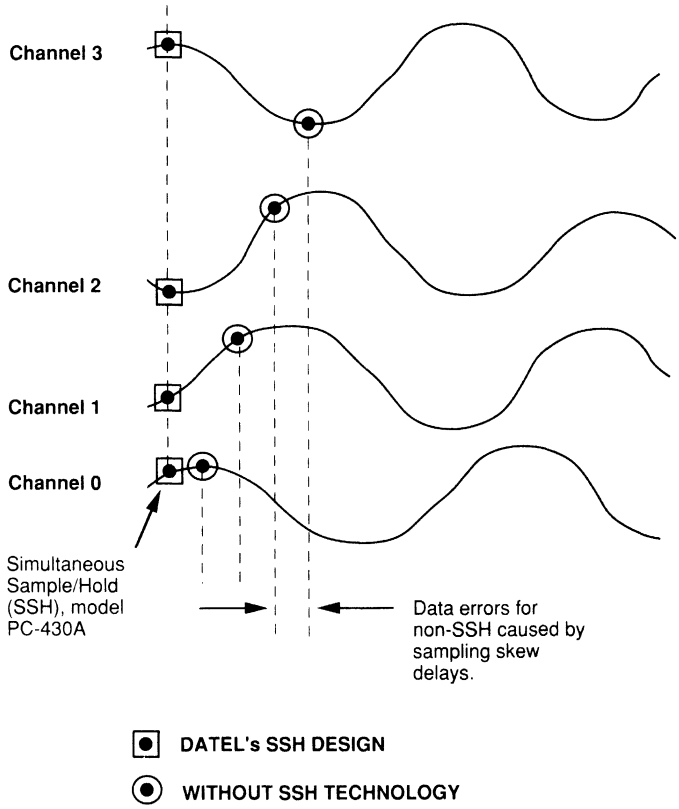


Figure 2. PC-430A Simultaneous Sample/Hold

FUNCTIONAL SPECIFICATIONS (Typical at +25 °C, dynamic conditions, gain=1, unless noted)

ANALOG INPUTS

Number of Channels	4 channels (430A,B,C) 1 channel (430D) 16S/8D channels (430E)
Input Configuration (A/D)	Single-ended, non-isolated on models PC-430A, PC-430B, PC-430C and PC-430D. The model PC-430E has 16S or 8 differential channels.

Full Scale Input Ranges	0 to +10V ±10V	±5V	±1.25V
(user-selectable) 430A	✔	-	-
[gain = 1] 430B	✔	✔	-
430C	✔	✔	-
430D	-	-	✔
430E	✔	✔	-

Programmable Gains (Model PC-430A only)	Programmable gain of 10 is selectable on 2 channels; 0 to +1V, ±1V [See Tech. Note 1]
Input Impedance [See Tech. Note 2]	10 Megohm, min. power on 50 ohm (D only) 1.5 Kilohms min. power off
Input Bias Current	± 1 nA
Input Capacitance	10 pF per channel
Input Overvoltage	± 15V (no damage)
O.V. Recovery Time	2 microseconds max.
Common Mode Volt. Range	±10V Max. (PC-430E)
Common Mode Rejection	-80 dB (PC-430E) dc to 60 Hz
Addressing Modes	1. Single channel 2. Simultaneous Sample/Hold 3. Sequential with autosequenced addressing 4. Random addressing by host software

SAMPLE/HOLD

Acquisition Time (FSR step) to 0.01% of FSR	750 nS max. (430A,E,B) 200 nS max. (430C) 50 nS max. (430D)
Aperture Delay	6 nS (430A) 30 nS (430B,C,E) 10 nS (430D)
Aperture Delay Uncertainty	±1 nS (430A) ±5 nS (430B,C,E) ±10 pS (430D)
Droop Rate	1 µV/µS
SSH Channel-to-Channel Linearity Tracking	± 0.03% (430A only)

A/D CONVERTER

Resolution	12 bits (430A,C,D,E) 14 bits (430B)
Conversion Period (A/D and S/H)	500 nanoseconds (430A) 1 microsecond (430B,C,E) 200 nanoseconds (430D)

A/D CONVERTER

Output Coding	Positive-true right-justified straight binary (unipolar) or right-justified two's complement (bipolar) with sign extension through bit 15.
Trigger Sources (Software selectable)	1. Local Pacer sample clock 2. External TTL sample clock

TOTAL SYSTEM CHARACTERISTICS

[See Tech. Note 3] **Integral Non-linearity**	±1 LSB of FSR (430A,C,E) ±1.5 LSB of FSR (430B,D)
Differential Non-linearity	± 0.75 LSB of FSR (430A,C,E) ± 1 LSB of FSR (430B,D)
Full Scale Temperature Coefficient	±0.1 LSB per °C (430A,C,D,E) ±0.3 LSB per °C (430B)
Zero or Offset Temperature Coefficient	±0.1 LSB per °C (430A,C,D,E) ±0.3 LSB per °C (430B)
Power Supply Rejection	±0.004% per % of bus +5V

A/D MEMORY

Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024 A/D samples, standard. Up to 4096 A/D samples (optional).

TOTAL SYSTEM DYNAMIC PERFORMANCE

System Bandwidth (single channel, half-scale input, to rated specifications)	1 MHz (430A,C) 200 KHz (430B,E) 2.5 MHz (430D)
Total Throughput to FIFO (single channel, gain=1)	700 nanoseconds (430A) 2 microseconds (430B,E) 1 microsecond (430C) 250 nS (430D)
Throughput to FIFO per A/D sample (sequential channels, gain = 1) [See Tech. Note 5]	1 microsecond (430A) 3 microseconds (430B) 2 microseconds (430C) 4 microseconds (430E)
Throughput to FIFO (sequential channels, gain = 10)	10 microseconds (430A)
Total Harmonic Distortion [See Tech. Note 6]	-72 dB (430A,C,E) -75 dB (430B) -68 dB (430D)

TRIGGER CONTROL

Programmable Timer/ Counter Type	82C54
Functions	1. EOC sample count 2. A/D start rate (16 bit divisor) 3. Scan trigger rate (16 bit divisor)
Pacer Sample Counter	1 to 65,536 samples. Drives the Acquire flag/interrupt gate for A/D start pulses.
Clock Source Internal External	 1. 8 MHz crystal clock 2. TTL input, user-selectable

PC/AT-BUS INTERFACE	
Architecture	I/O and memory mapped, for IBM-PC/AT, PS-30, EISA bus and compatibles.
I/O Mapping	Decodes two 8-bit I/O registers. Decodes I/O address lines A9-A2. 3F0H maximum.
Data Transfer	Memory block transfer or host DMA, software selectable.
Data Bus	16 bits.
Direct Memory Access	1 channel, selectable on chanels 5, 6 or 7
DMA Request Conditions (software selectable)	FIFO full, half full, not empty, scan acquire flag (sample count) or user programmable.
Control/Status Functions	Board reset, FIFO flags, interrupt select and status, DMA select and status, trigger source, timer control and period, sample count load, A/D enable, MUX auto-sequence, DSP hold/ack, DPR enbl/dsbl.
Number of Interrupts	1 interrupt, selectable on levels 7, 9 thru 12, or 15.
Bus Interrupt Sources	DSP interrupt request to PC or DMA terminal count from bus.

LOCAL MICROCOMPUTER	
CPU Type	TI TMS 320C30 with internal DMA.
Local Data Bus	32 bits
CPU Clock Speed	32.000 MHz
Local DMA Controller	Internal to 320C30 CPU
Primary Memory (Dual ported to PC/AT)	128K x 32 static RAM
Expansion Memory	8K x 32 static RAM
Internal DSP Memory	Two 1K x 32
Dual Port Access	Hold mode by control bit or from PC/AT dynamic hold per each access.
CPU Test Port	Supports TI XDS1000 Extended Development System.
Local Interrupts	Int 0-3 from PC host request, A/D FIFO or acquire flags or optional external interrupt.

MISCELLANEOUS	
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain per channel for SSH on PC-430A. A single offset and gain pot is provided on PC-430B, C, D, and E.
Analog Input Connectors	Four miniature threaded coaxial, type SMA, mounted on rear slot. DB-25 for 430E
Trigger Connector	5th SMA for external TTL trigger. (A - D only)
I/O Expansion Port, P2	Dual-row header connector for 320C30 I/O (unbuffered).
Memory Expansion Port, P3	Dual-row header connector for 320C30 memory (unbuffered).

MISCELLANEOUS (continued)	
Serial Port and External Trigger/Pacer Clock,P1	Two serial channels, Compatible to 320C30 serial ports. Both scan (Trigger) and A/D sample (Pacer) clocks are accepted at connector. Dual-row header.
RS-232-C Serial Port	3 header pins. Uses software UART.
Operating Temp. Range	0 °C to +60 °C
Storage Temp. Range	-25 °C to +85 °C
Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet. Forced cooling is recommended.
Power Required	+5V dc at 3.5 Amps maximum from AT bus.
Outline Dimensions	4.2 x 13.2 inches, compatible to PC/AT bus.

TECHNICAL NOTES

[1] Resistor-programmed gain from x1 to x100 is available on PC-430E with increased settling delay at higher gain.

[2] The input impedance of 10 megohms minimum avoids attentuation errors from external input source resistance. For many applications, an inline coaxial 50Ω shunt, inserted adjacent to the front connectors, is recommended to reduce line reflections and standing wave errors.

[3] Allow 20 minutes warmup time to rated specifications for model PC-430B.

[4] Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

[5] The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the PC-430C were scanned, the maximum sample rate on any one channel would be 2 microseconds X 4 channels = 8 microseconds (125 KHz per channel).

[6] THD test conditions are:

1. Input frequency:
   500 KHz (PC-430A)
   200 KHz (PC-430B, and PC-430E)
   300 KHz (PC-430C)
   1 MHz (PC-430D)
2. Generator/filter THD is -90 dB minimum.
3. THD computed by FFT to 5th harmonic.

$$THD = 20 * \log 10 \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{V_{IN}}$$

4. Inputs are 1/2 full scale. No channel advance.
5. A/D trigger rate:
   1.5 MHz (PC-430A)
   500 KHz (PC-430B, PC-430C, and PC-430E)
   4 MHz (PC-430D)

PC-430 Software

The PC-430 system has been designed to optimize three competing objectives:

- Easy to use (no local programming)
- Fast
- Powerful (access to full DSP library)

To achieve these mutually exclusive goals, a high speed command list form of control is used. The Application Function Block (AFB) is a short list calling local library functions. No local programming is needed. The user writes the AFB file with any text editor and it is then converted on the PC side to an internal binary form. The converted AFB is then downloaded to PC-430 Dual Port RAM (DPR) and executed. The AFB is powerful because of full access to the local DSP library and because repeating functions may be looped. These loops in turn may be nested. Loops can run with a loop count or "forever" until stopped.

Unlike a slow ASCII interpreter, the AFB runs at the full speed of the 320C30 DSP with minimal overhead. And to accept fast A/D's without sample loss, only a fully integrated hardware/software system will handle the bandwidth. This hardware system consists of local FIFO A/D memory, local FIFO interrupts and a local Direct Memory Access (DMA) controller inside the DSP which runs in background. FIFO interrupts cause DMA data block transfers while the DSP continues foreground processing.

Executive Package

The complete Executive Software Package is an integrated environment for full control of the PC-430. It includes programs which run on both the host PC and the PC-430. The Executive Software Package consists of:

- The AFB ASCII to binary file converter (AFBCNVRT)
- A small menu shell
- The PC Host Driver/ User Interface
- The Executive scheduler, DSP library, boot code, vectors, and full local PC-430 system.

To use this environment, the user simply converts the AFB text file to a binary file, downloads this to the PC-430 through the Driver and retrieves data files.

PC-430 Host System Architecture

(See Figure 4)

When the PC-430 is fully installed, the host PC memory map contains the resident library, the Interrupt Service Routine, a small menu program and the PC-430's dual port RAM. These systems all work together to provide fast disk or buffer transfers of DSP'd A/D data. The entire system is controlled by simple user-written command files.

Software Hierarchy

The relationship between software in the PC host and in the PC-430 is illustrated in this diagram. Control flows downward from the user's AFB and A/D data flows upward. See Figure 3.

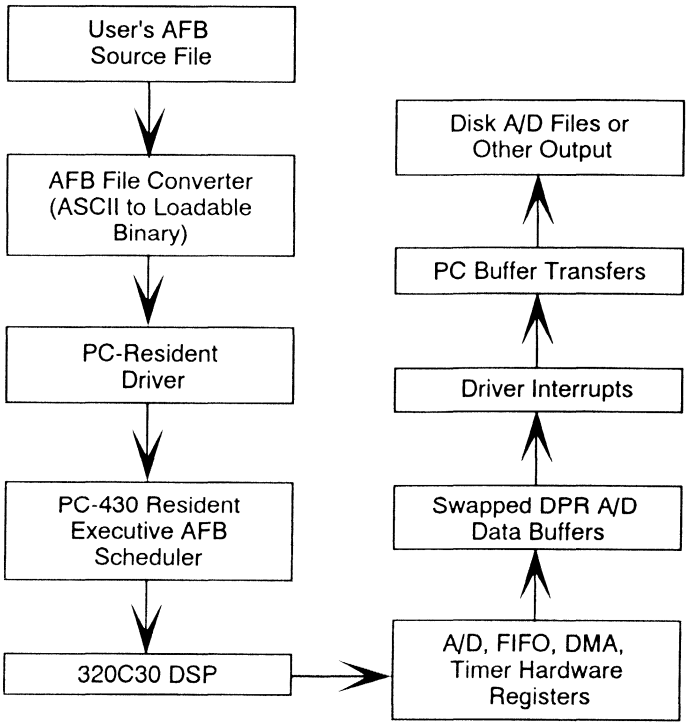


Figure 3. Software Hierarchy Flow Chart

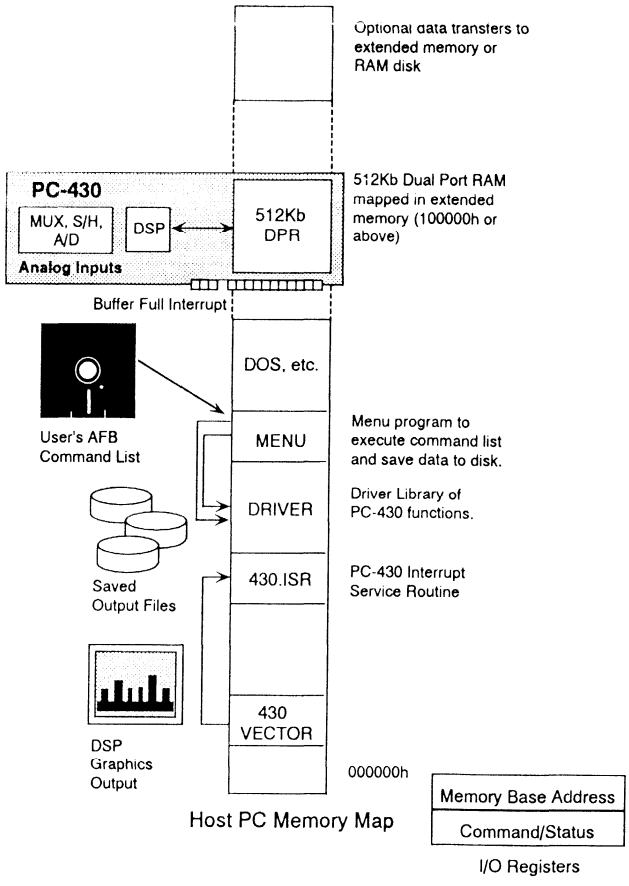


Figure 4. PC-430 Host System Architecture

Library Functions

The following functions are downloaded at power up by the Driver to the PC-430 DPR and form the resident on-board DSP library. They may be called from the DPR by including them in the user's downloaded AFB.

A/D Scan Routines

initad	Initialize the start channel address.
inittim0	Initialize timer 0
inittim1	Initialize timer 1
inittim2	Initialize timer 2
sadtsc	Select internal or external A/D trigger source.
sadcr	Select the A/D internal conversion rate.
sstr	Select the internal scan trigger rate.
sadspc	Select the number of A/D samples.
stads	Set the total number of A/D samples under 65K. (For 65K or greater, refer to the special techniques in the user manual.)
sfifoi	Enable or disable local FIFO interrupts.
sadr	Enable or disable A/D conversions.
rfifo	Reset FIFO.
calad	Calibrate A/D single samples.
fifoisr	FIFO local interrupt service routine.
scommreg	Set A/D command register.

DSP Array Routines

fir	Do FIR filter on array with user-supplied coefficients.
iir	Do IIR filter on array with user-supplied coefficients.
linfir	Convolution on linear array.
cirfir	Convolution on circular array.
windham, windhan	Multiply a Hamming or Hanning window with signal data array.
windrec	Multiply a rectangular window with a signal data array.
windblh	Multiply a Blackman-Harris window with signal data array.
windrco	Multiply a Raised Cosine window with signal data array.
cfftc	Do complex Fast Fourier Transform (FFT) on array.
fft	Do real FFT on array.
bitrev	Generate complex array of bit-reversed twiddle factors.
twiddle_r	Generate array of twiddles for real FFT.
dct	Do Discrete Cosine Transform on array (for signal compression).
magfft	Calculate magnitude of real FFT array.
dbfft	Perform log10 on FFT array to prepare data for graphic display.
call sine, call cos	Generate sine or cosine arrays.
call const	Fill array with constant.

PC-430 I/O Registers

I/O Address	Direction	Function
I/O BASE + 0	Write	PC Command Register
	Read	PC Status Register
I/O BASE + 2	Write	Memory Base Address
	Read	Not Used

Command Register
(Write I/O BASE + 0)

PC Interrupt Level Enable [Bits 2 - 0]
DMA Enable/Disable [Bits 4, 3]
DSP Interrupt Request [Bit 5]
DSP Hold Request [Bit 6]
DSP Reset/Run [Bit 7]
[Bits 15 - 8 Are Not Used].

Status Register
(Read I/O BASE + 0)

Bits 5 - 0 and 15 - 8 are not used.
DMA Terminal Count Status [Bit 6]
DSP Hold Acknowledge [Bit 7]

Memory Base Address Register
(Write Only To I/O BASE + 2)

Bits 1, 0 and 15 - 8 are not used.
Memory Enable/Disable [Bit 2]
BASE Address, LA23 - 19 [Bits 7 - 3]

Array Conversion Routines

The 320C30 DSP uses an internal 32-bit floating point format which is optimized for hardware speed.

ieeedsp	Convert IEEE-754 floating point array to 320 format.
dspieee	Convert 320 array to IEEE-754 floating point format.
matadd	Doubleword matrix addition on array.
matmul	Doubleword matrix multiplication on array.
hstgrm	Histogram of doubleword array.
int2flt	Convert doubleword integer array to 320 floating point.
sign_extend	Extends polarity bit from 15 to 31.

Single Variable Transcendentals

sine, cosine, tangent
hyperbolic sine, cosine, tangent
inverse sine, cosine, tangent
square root, powers, exponential
natural logarithm, Base10 logarithm

These functions are available in the TI "C" compiler library.

Buffer Management

defsbuf, defdbuf	Define single and double buffers.
set ibuf, set obuf	Setup input and output double buffers. Post current buffer addresses in Exec status area. Used for non-stop A/D filling without sample loss. Interrupt PC.
unrav2, unrav4	Separate one array of sequential multichannel data into two or four single channel arrays.
concat	Compress an array of one A/D sample per 32-bit longword into an array of contiguous 16-bit A/D words. Concat forms a single 32-bit longword from the 16-bit LSB's of two longwords. MSB's are discarded.
switch_buffers	Swap double buffers.
ibuf_ready ibuf_release	Input buffer transfer handshakes.
pause	Momentarily stop AFB execution to allow PC access for table upload/download
dprxfer	Do block transfers within PC-430 local memory between buffers using buffer numbers.
addxfer	Do block transfers within PC-430 local memory between absolute addresses. Overlapped transfers will preserve data.
int2pc	Select buffer ready or local timer interrupt to PC.

PC-Resident Driver Interface

The final portion of the full Executive package is the User Interface and Driver containing a library of functions to control the PC-430. This program offers a simple menu to control the PC-430. No programming is required.

The Driver functions are:

- Install PC Interrupt Service Routine (ISR) to respond to PC-430 buffer full flags.
- Initialize the PC interrupt and DMA systems.
- Set the PC-430 extended memory base address and test memory.
- Download the Exec, library and full local system to the PC-430 DPR from a system binary file.
- Boot the local PC-430 system and confirm.
- Allocate a PC Host buffer to receive PC-430 data.
- Download a converted AFB file and start execution.
- Collect data to buffer or disk using swapped double buffer interrupts. (Extended memory block transfers to a user-defined buffer may also be selected.)
- Stop the AFB and save the PC-430 data buffer to a file.
- Load and run a user COFF object file.
- Calibrate the A/D. Halt and reset the DSP. Quit to DOS.

Resident Debugger/Monitor

For users who prefer more direct control of the PC-430 instead of the AFB, optional user programs written in TI "C" or 320C30 assembly language may be run after downloading from the host. Once debugged, local executable code may be loaded into a PROM which replaces some of the on-board RAM. Or the user may simply retain the download method.

An integrated windowed package consisting of the Debugger (on the PC-430 side) and the Monitor (on the host PC side) offers the following functions:

- Load TI COFF-format object file.
- Display or modify memory (in hex, decimal integer, ASCII, or TI/IEEE floating point).
- Display or modify CPU registers.
- Disassemble memory.
- View file.
- Set, display, or remove breakpoints.
- Go from address until optional breakpoint.
- Single Step DSP, Halt/reset DSP, Block fill.
- Shell out to DOS, Quit to DOS.

AFB Source File Format

The AFB source format uses symbolic names for internal PC-430 library functions. The C-like file may be written in free form with the user's choice of loop nesting indentation, skipped lines, etc. Comments after the function name delimiter are ignored. After the user writes the AFB, the AFBCNVRT file converter prepares a binary output file which is subsequently downloaded through the Driver for execution.

Here is an AFB example which defines buffers, generates a sine wave, then prepares an FFT array for floating point output:

```
DEFDBUF,          ;function to define double buffer
  0x0L,           ;starting buffer number
  0x400L,         ;buffer length
  0x200L,         ;alignment
DEFSBUF,          ;define single buffer
  0x2L,           ;buffer number
  0x100L,         ;buffer length
  0x100L,         ;alignment
TWIDDLE_R,        ;generate twiddle factors
  0x2L,           ;buffer number 2
BEGIN,            ;begin loop flag
  FOREVER         ;-1 = loop forever flag
CALL_SINE,        ;fill buffer with sine array
  0x00000000L,    ;buffer number 0
  0x00000020L,    ;period of the sine wave
FFT,              ;do FFT on buffer
  0x0L,           ;buffer number 0
  0x200L,         ;number of points
  0x9L,           ;Log 2 of number of points
  0x2L,           ;buffer for twiddle factors
MAGFFT,           ;take magnitude of FFT data
  0x0L,           ;buffer number 0
  0x200L,         ;FFT size
DSPIEEE,          ;convert to IEEE format
  0x0L,           ;buffer number 0
  0x100L,         ;buffer length
SET_OBUF,         ;signal to PC that buffer is ready
  0x0L,           ;buffer 0
  0x100L,         ;buffer length
SWITCH BUFFERS,   ;swap double buffers
END               ;loop back to BEGIN
```

ORDERING GUIDE

Model	A/D Bits	FIFO Size (Samples)	Channels	Sample Rate Single Channel	Simultaneous Sample/Hold	PGA
PC-430A1	12	1K	4	1.5 MHz	4 channels	x1,x10
PC-430A2		4K				
PC-430B1	14	1K	4	500 KHz	none	none
PC-430B2		4K				
PC-430C1	12	1K	4	1 MHz	none	none
PC-430C2		4K				
PC-430D1	12	1K	1	4 MHz	none	none
PC-430D2		4K				
PC-430E1	12	1K	16S/8D	500 KHz	none	x1 to x100
PC-430E2		4K				(Resistor select)

Each board is power-cycle burned-in, tested and calibrated. All models include a user's manual. The warranty period is one year.

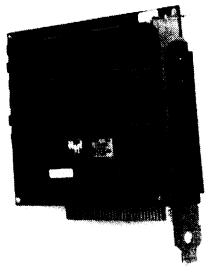
Software:

PC-430EXEC	Executive, driver, and command converter program, 3.5" and 5.25" MS-DOS disks
PC-430BUG	Monitor/Debugger, MS-DOS disks
61-7342340	SMA male to BNC male coaxial cable, 1 meter length (1 cable required per channel)
PC-430HYPER	Hyperception integrated control/store/display program

PC-DIO-96
96 Channel Digital I/O Board for IBM-PC/XT/AT

FEATURES

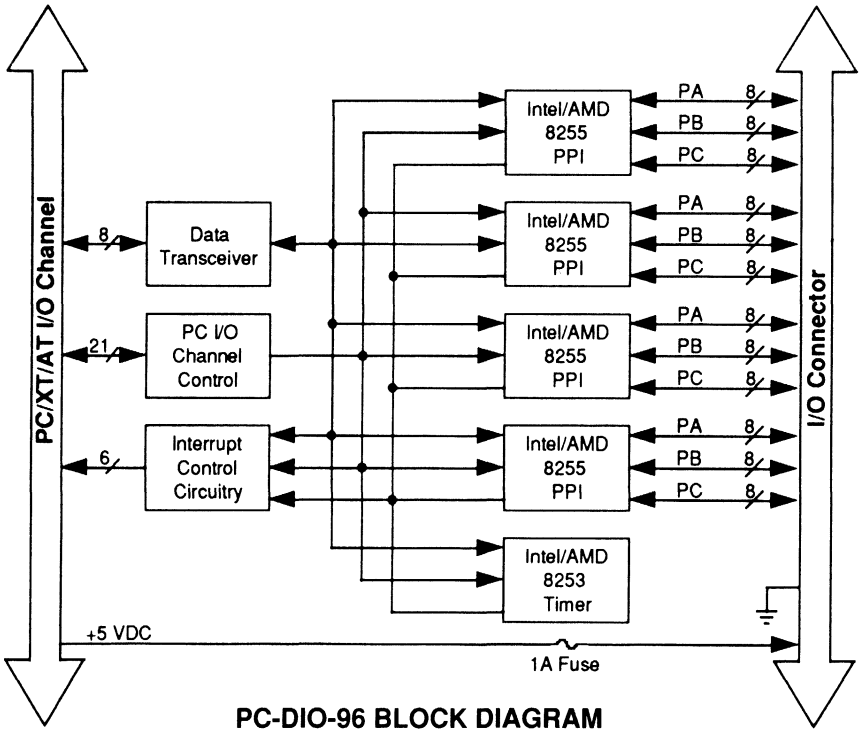
- **96 parallel (TTL Level) bits in 12 x 8-bit ports**
- **Programmable interval timer (for up to 6 periodic CPU interrupts)**
- **Update/Transfer Rates to 460 Kbytes/sec (maximum)**
- **100% Compatible with LabWindows Software Package**
- **Independent bidirectional ports for Sense/Control Applications**
- **Uses 4 x 8255A programmable peripheral interface ICs**
- **Delivery from stock! Very low cost!**



GENERAL DESCRIPTION

DATEL's PC-DIO-96 is a high performance, low cost 96 channel parallel I/O board for IBM-PC/XT/AT and compatible personal computers. The 96 channels are arranged in 4 x 24-bit ports (using 4 Intel/AMD 8255's) that may be further divided into 12 x 8-bits ports. Each port may be independently programmed for either input or output for complex, discrete monitoring and control applications often found in industry and research laboratories. The half size board is bus compatible with both the IBM-PC/XT and IBM-PC/AT and provides for periodic interrupt capability via a sophisticated Programmable Interval Timer.

All channel control circuitry including channels latches, address decoding, data buffers and interface timing and control are built into the PC-DIO-96 so that you need not be concerned with writing complex control software. However, it's flexible design allows the experienced programmer direct access to all 12 (8-bit) ports for direct port manipulation/control. The programmable interval timer may also be accessed for generating periodic interrupt requests (priority level set via jumpers) to the CPU. The 2 MHz clock of the timer may be reduced via 16 or 32-bit dividers allowing interrupt generation from 20 µsec to 35 minutes. All input and output data is buffered to and from the CPU via an on-board data transceiver. PC-DIO-96 data transfer (programmed I/O) is done in 8-bit segments, via the transceiver, at a rate of 460 Kbytes/sec (tested on Compaq Systempro 386/33). All lines are TTL compatible with drive current (Darlington) of -4.0 mA (-1.0 mA, minimum). Power consumption is a very low 5V dc (at 0.45A, typical). All I/O signals (and 5V dc output power) are available at a 100 pin header (with optional, removable ribbon cable and dual screw terminal connector blocks) for easy access.



PC-DIO-96 BLOCK DIAGRAM

APPLICATIONS

- **Controller for Centronics Printers**
- **Interface for Industry Standard Solid State Relay Modules**
- **High Density Mixed Digital I/O Acquisition/Control Schemes**
- **BCD Input or Output from Digital Panel Meters, etc.**
- **High Speed, Digital Test Pattern Generator**
- **Status Monitor for Contact Closures, Relays, Solenoids, etc.**

The PC-DIO-96 is fully compatible with LabWindows, an auto-code generating, menu-driven software package for data acquisition and analysis. The PC-DIO-96 may also be programmed directly from other languages such as Microsoft C and QuickBASIC, etc.

It's compact size, low cost and high performance make the PC-DIO-96 the perfect choice for interfacing to printers, instruments (BCD format), panel meters, and other peripherals as well as high density mixed digital I/O signals, monitoring contact closures, and higher power ON/OFF control schemes when used with solid state relay modules from OPTO 22, P&B, etc.

HARDWARE CAPABILITY

Programmable Peripheral Interface (PPI)

The PC-DIO-96 is designed around four 8255A PPIs consisting of 4 x 24-bit parallel digital I/O lines. Each PPI contains 3 x 8-bit parallel ports programmable as either inputs or outputs on a per port basis. Ports A & B are used for byte-wide digital I/O while port C is capable of 4-bit (or 8-bit) I/O and may be used for digital data I/O, control lines, status monitoring, or as handshake lines for external peripherals. The PC-DIO-96 can be programmed for unidirectional or bidirectional I/O.

Data Transceiver

All data is buffered to and from the PCbus via a data transceiver. This is an 8-bit wide transceiver that latches data from the PC-DIO-96 to and from the IBM-PC/XT/AT.

Programmable Interval Timer

The PC-DIO-96 has an on-board programmable interval timer capable of generating periodic interrupts to the computer CPU. The programmable interval timer employs a high speed 8253 counter/timer clocked at 2 MHz to generate the interrupt request. Interrupt priority levels/lines are set via jumper switches on the main board. The output rate of the 8253 is reduced using 16 or 32-bit dividers yielding interrupts request rates from 20 µsec to 35 minutes.

Interrupt Control Circuitry

Interrupt requests may be generated by the 8255A via lines PC0 or PC3 of the lower 4-bits of Port C for one-shot requests or by counter 0 and 1 of the programmable interval timer for repetitive interrupt requests from 20 µsec to 35 minutes periods. One of six interrupt request lines may be selected via on-board jumpers and associated with interrupt levels in software. A master enable bit controls interrupt requests in software.

Signal I/O Connector

All signals are terminated at a 100-pin male header with optional ribbon cable and dual screw terminal boards for easy signal I/O. Port A for each of the 4 PPIs is shown in the connector pinout (below) as xPA7 through xPA0 and designated as A, B, C, or D for the four PPIs. Ports B and C for each PPI are similarly designated using xPB7, xPC7, etc. Each port may be configured via software) as either input or output and may be changed at any time. +5V dc from the IBM-PC/XT/AT is also available via pins 49 and 99 of the I/O header.

SOFTWARE SUPPORT

The PC-DIO-96 is fully supported by LabWindows 2.0. LabWindows is an icon-based set of software tools capable of automatic code generation for virtually any data acquisition and control board or system. Not limited to data collection alone, LabWindows will graphically display your collected data and is available with a powerful data analysis package supporting a math coprocessor (not required) for FFT, FHT, integration/differentiation, linear equations, Polynomial curve-fitting, Statistics, Butterworth and Chebyshev digital filters, power spectrum analysis, etc.

LabWindows employs Microsoft C and QuickBASIC compatible libraries for maximum speed and versatility. Pull down menus and Icon-based user interface make this package a breeze to use. Also included with LabWindows is an huge library for support of many common industrial/laboratory instruments using RS-232, GPIB, data acquisition boards, etc. LabWindows may also be used as a stand alone data analysis and graphics package for data collected from any source including keyboard entered data.

SPECIFICATIONS

(All specifications are typical at 25 °C unless otherwise noted)

DIGITAL I/O LINES

Input Logic (low)
- Minimum 0V
- Maximum 0.8V

Input Logic (high)
- Minimum 2.0V
- Maximum 5.25V

Output Logic (low)
- at 1.7 mA, minimum 0V
- at 1.7 mA, maximum 0.45V

Output Logic (high)
- at -200 µA, minimum 2.4V
- at -200 µA, maximum 5.0V

Input Load Current
- (0 < Vin < 5V), minimum ..... -10 µA
- (0 < Vin < 5V), maximum ..... 10 µA

Darlington Drive Current
- (R ext = 750 Ohms, V ext = 1.5V)
  - Minimum ..... -1.0 mA
  - Maximum ..... -4.0 mA

DATA TRANSFER RATE

Programmed I/O
- (Using 8 MHz IBM PC/AT) ..... 300 Kbytes/sec

POWER CONSUMPTION

+5V dc, typical ..... 0.16 A

PHYSICAL

Dimensions ..... 3.9" x 6.5"
I/O Connector ..... 50-pin, male ribbon cable connector

ENVIRONMENTAL

Operating Temperature ..... 0 °C to +70 °C
Humidity (non-condensing) ..... 5% to 90%
Storage Temperature ..... -55 °C to +150 °C
Noise Emission ..... FCC Class A verified (shielded ribbon cable)

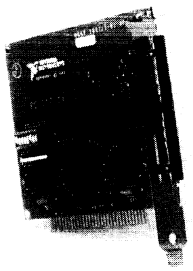
PC-DIO-96 I/O CONNECTOR

APC7	1	51	CPC7
BPC7	2	52	DPC7
APC6	3	53	CPC6
BPC6	4	54	DPC6
APC5	5	55	CPC5
BPC5	6	56	DPC5
APC4	7	57	CPC4
BPC4	8	58	DPC4
APC3	9	59	CPC3
BPC3	10	60	DPC3
APC2	11	61	CPC2
BPC2	12	62	DPC2
APC1	13	63	CPC1
BPC1	14	64	DPC1
APC0	15	65	CPC0
BPC0	16	66	DPC0
APB7	17	67	CPB7
BPB7	18	68	DPB7
APB6	19	69	CPB6
BPB6	20	70	DPB6
APB5	21	71	CPB5
BPB5	22	72	DPB5
APB4	23	73	CPB4
BPB4	24	74	DPB4
APB3	25	75	CPB3
BPB3	26	76	DPB3
APB2	27	77	CPB2
BPB2	28	78	DPB2
APB1	29	79	CPB1
BPB1	30	80	DPB1
APB0	31	81	CPB0
BPB0	32	82	DPB0
APA7	33	83	CPA7
BPA7	34	84	DPA7
APA6	35	85	CPA6
BPA6	36	86	DPA6
APA5	37	87	CPA5
BPA5	38	88	DPA5
APA4	39	89	CPA4
BPA4	40	90	DPA4
APA3	41	91	CPA3
BPA3	42	92	DPA3
APA2	43	93	CPA2
BPA2	44	94	DPA2
APA1	45	95	CPA1
BPA1	46	96	DPA1
APA0	47	97	CPA0
BPA0	48	98	DPA0
+5V	49	99	+5V
GND	50	100	GND

PC-DIO-24
24 Channel Digital I/O Board for IBM-PC/XT/AT

FEATURES

- **24 parallel (TTL Level) bits in 3 x 8-bit ports**
- **Update/Transfer Rates to 300 Kbytes/sec maximum**
- **100% compatible with LabWindows software package**
- **Independent bidirectional ports for sense/control applications**
- **Uses 8255 Programmable Peripheral Interface (PPI)**
- **Delivery from stock! Very low cost!**

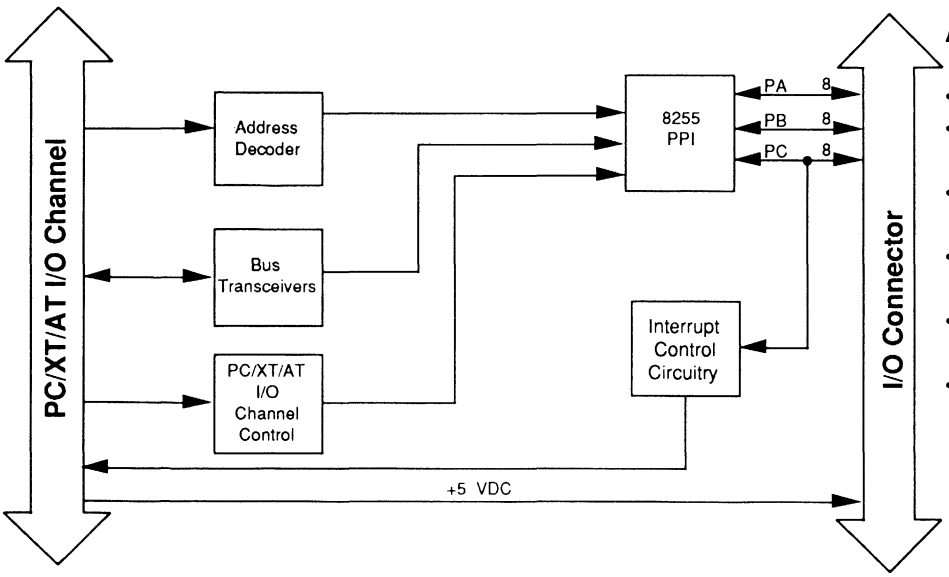


GENERAL DESCRIPTION

DATEL's PC-DIO-24 is a high performance, low cost 24 channel parallel I/O board for IBM-PC/XT/AT and compatible personal computers. The 24 channels are arranged in 3 x 8-bit ports (using Intel/AMD 8255). Each port may be independently programmed for either input or output for complex, discrete monitoring and control applications often found in industry and research laboratories. The half size board is bus compatible with both the IBM-PC/XT and IBM-PC/AT and provides for periodic interrupt capability via a sophisticated Programmable Interval Timer.

All channel control circuitry including channels latches, address decoding, data buffers, and interface timing and control are built into the PC-DIO-24 so that you need not be concerned with writing complex control software. However, its flexible design allows the experienced programmer direct access to all three (8-bit) ports for direct port manipulation/control. Interrupt requests may be generated via the 8255 on any of six interrupt lines. All input and output data is buffered to and from the CPU via an on-board data transceiver. PC-DIO-24 data transfer (programmed I/O) is done in 8-bit segments, via the transceiver, at a rate of 300 Kbytes/sec (tested on 8 MHz IBM PC/AT). All lines are TTL compatible with drive current (Darlington) of -4.0 mA (-1.0 mA, minimum). Power consumption is a very low 5V dc (at 0.16 A, typical). All I/O signals (and 5V dc output power) are available at a 50 pin header (with optional, removable ribbon cable and dual screw terminal connector blocks) for easy access.

The PC-DIO-24 is fully compatible with the LabWindows, an auto-code generating, menu-driven software package for data acquisition and analysis. The PC-DIO-24 may also be programmed directly from other languages such as Microsoft C and QuickBASIC, etc. It's compact size, low cost and high performance make the PC-DIO-24 the perfect choice for interfacing to printers, instruments (BCD format), panel meters, and other peripherals as well as high density mixed digital I/O signals, monitoring contact closures, and higher power ON/OFF control schemes when used with solid state relay modules from OPTO 22, P and B, etc.



PC-DIO-24 BLOCK DIAGRAM

APPLICATIONS

- **Controller for Centronics Printers**
- **Interface for Industry Standard Solid State Relay Modules**
- **High Density Mixed Digital I/O Acquisition/Control Schemes**
- **BCD Input or Output from Digital Panel Meters, etc.**
- **High Speed, Digital Test Pattern Generator**
- **Status Monitor for Contact Closures, Relays, Solenoids, etc.**

HARDWARE CAPABILITY

Programmable Peripheral Interface (PPI)

The PC-DIO-24 is designed around a single 8255 PPI consisting of a 24-bit parallel digital I/O lines. The PPI contains 3 x 8-bit parallel ports programmable as either inputs or outputs on a per port basis. Ports A and B are used for byte-wide digital I/O while port C is capable of 4-bit (or 8-bit) I/O and may be used for digital data I/O, control lines, status monitoring, or as handshake lines for external peripherals. The PC-DIO-24 can be programmed for unidirectional or bidirectional I/O.

Address Decode

The Base address for the PC-DIO-24 is set via a single 8-gang DIP switch. Address decode circuitry is built in the PC-DIO-24 for direct access to the 8255. This allows easy access to all 8255 functions.

PC/XT/AT I/O Channel Control

PC/XT/AT I/O channel control circuitry receives bus signals to control PC-DIO-24 operation. These channel control signals specify the type of bus cycle in progress. Bus cycles can be either memory or I/O, read or write and can transfer 8-bit data.

Data Transceiver

All data is buffered to and from the PC bus via a data transceiver. This is an 8-bit wide transceiver that latches data from the PC-DIO-24 to/from the IBM-PC/XT/AT.

Interrupt Control Circuitry

Interrupt requests may be generated by the 8255 via lines PC0 or PC3 of the lower 4-bits of Port C for simple, one-shot interrupt requests. One of six interrupt lines may be selected via a 2 x 6 on-board jumper and associated with interrupt enable signals being generated (jumpers) from PC2, PC4, or PC6.

Signal I/O Connector

All signals are terminated at a 50-pin male header with optional ribbon cable and screw terminal board for easy signal I/O. Port A is shown in the connector pinout as PA7 through PA0. Ports B and C are similarly designated using PB7 and PC7. Each port may be configured (via software) as either input or output and may be changed at any time. +5V dc from the IBM-PC/XT/AT is also available at pin 49 of the I/O header.

PC-DIO-24 I/O CONNECTOR

PC7	1	2	GND
PC6	3	4	GND
PC5	5	6	GND
PC4	7	8	GND
PC3	9	10	GND
PC2	11	12	GND
PC1	13	14	GND
PC0	15	16	GND
PB7	17	18	GND
PB6	19	20	GND
PB5	21	22	GND
PB4	23	24	GND
PB3	25	26	GND
PB2	27	28	GND
PB1	29	30	GND
PB0	31	32	GND
PA7	33	34	GND
PA6	35	36	GND
PA5	37	38	GND
PA4	39	40	GND
PA3	41	42	GND
PA2	43	44	GND
PA1	45	46	GND
PA0	47	48	GND
+5V dc	49	50	GND

SOFTWARE SUPPORT

The PC-DIO-24 is fully supported by National Instruments Lab-Windows 2.0. LabWindows is an icon-based set of software tools capable of automatic code generation for virtually any data acquisition and control scheme. Not limited to data collection alone, LabWindows will graphically display your collected data and is available with a (optional) powerful data analysis package supporting a math coprocessor (not required) for FFT, FHT, integration/differentiation, linear equations, Polynomial curve-fitting, Statistics, Butterworth and Chebyshev digital filters, power spectrum analysis, etc.

LabWindows employs Microsoft C and QuickBASIC compatible libraries for maximum speed and versatility. Pull down menus and Icon-based user interface make this package a breeze to use. Also included with LabWindows is an huge library for support of many common industrial/laboratory instruments using RS-232, GPIB, data acquisition boards, etc. LabWindows may also be used as a stand alone data analysis and graphics package for data collected from any source including keyboard entered data.

DATEL also offers a second, low cost, library of functions supporting the PC-DIO-24 from Microsoft C or QuickBASIC. The routines (functions) in PC LabDriver are callable from both of the above languages for simple, fast applications specific programs.

SPECIFICATIONS

(All specifications are typical at 25 °C unless otherwise noted)

DIGITAL I/O LINES

Input Logic (low)
- Minimum 0V
- Maximum 0.8V

Input Logic (high)
- Minimum 2.0V
- Maximum 5.25V

Output Logic (low)
- at 1.7 mA, minimum 0V
- at 1.7 mA, maximum 0.45V

Output Logic (high)
- at -200 µA, minimum 2.4V
- at -200 µA, maximum 5.0V

Input Load Current
- (0 < Vin < 5V), minimum ..... -10 µA
- (0 < Vin < 5V), maximum ..... 10 µA

Darlington Drive Current
- (R ext = 750 Ohms, V ext = 1.5V)
  - Minimum ..... -1.0 mA
  - Maximum ..... -4.0 mA

DATA TRANSFER RATE

Programmed I/O
- (Using 8 MHz IBM PC/AT) ..... 300 Kbytes/sec

POWER CONSUMPTION

+5V dc, typical ..... 0.16 A

PHYSICAL

Dimensions ..... 3.9" x 6.5"
I/O Connector ..... 50-pin, male ribbon cable connector

ENVIRONMENTAL

Operating Temperature ..... 0 °C to +70 °C
Humidity (non-condensing) ..... 5% to 90%
Storage Temperature ..... -55 °C to +150 °C
Noise Emission ..... FCC Class A verified (shielded ribbon cable)

LabWindows 2.0
PC/XT/AT Menu-Driven Data Acquisition Software

FEATURES

- **IBM-PC/XT/AT snd PS-2 compatible**
- **Supports DIO-24/96, TIO-10, AT-GPIB, GPIB-II/IIA**
- **Dramatically cuts programming time**
- **Automatic code generation (C or QuickBASIC)**
- **Powerful, full screen graphics**
- **Complex, sophisticated data analysis**
- **FFT and wave form analysis**
- **High speed data throughput**
- **Extensive IEEE-488, RS-232 support**
- **ON-line debugging, editing, and execution**
- **Executes under standard DOS**

GENERAL DESCRIPTION

LabWindows 2.0 is a unique software package allowing interactive, menu-driven program development and automatic code generation for even the most complex data collection, analysis, control, and display applications. Sparkling graphics, high speed data streaming, and complex data analysis routines may be designed and executed with minimal programming!

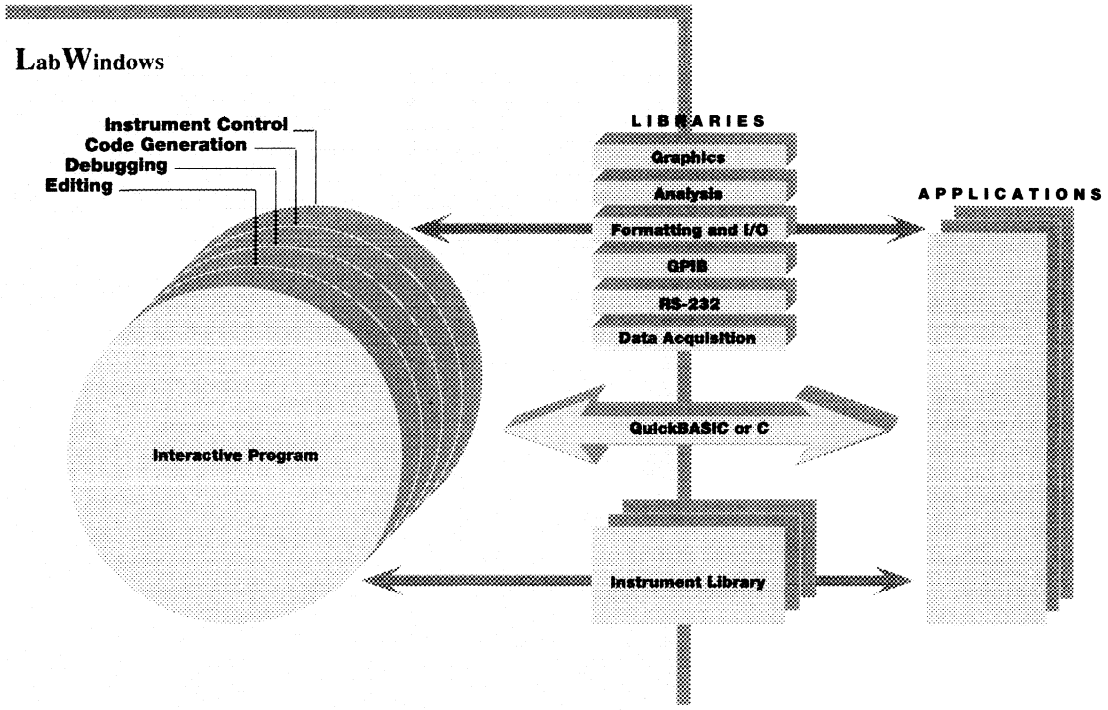
LabWindows 2.0 can perform virtually any data acquisition & control job in a fraction of the time spent developing your own programs. From Fast Fourier Transforms, complex waveform analysis and data capture from boards and instruments to data entered from the keyboard, LabWindows 2.0 saves time and money.

LabWindows is designed using pull down menus for fast, easy point and execute code generation. Also supplied are extensive analysis libraries, full screen graphics and wide support for the digital I/O, counter/timer, and GPIB cards carried by DATEL.

LabWindows is not tied to any specific I/O board or data acquisition subsystem (many of the included libraries use specific boards) so that this one package may be used with existing hardware and future upgrades without compatibility worries. In fact, LabWindows may be used to analyze and display data entered from the keyboard or gathered over your computers serial or GPIB port from other instruments.

APPLICATIONS

- **Complex waveform analysis**
- **High speed data acquisition and control**
- **Menu-driven program development**
- **Multiple order curve-fitting**
- **Statistics data analysis**
- **Graphic display of data**



QuickBASIC or C Compatible Programming

LabWindows 2.0 gives you interactive tools allowing development of application programs using a subset of Microsoft QuickBASIC and C programming languages. This allows programs to be developed and executed from LabWindows as well as saving the program modules in ASCII text files for later, stand-alone compilation and execution. As a result, all existing software tools retain their value. The extensive application libraries are included as both executable and object files for linking to your stand-alone application programs. A special screen oriented utility makes linking stand-alone programs as easy as filling in the blanks.

Editing and Debugging

LabWindows pull down menus and mouse interface gives you easy, direct access to many editing and debugging functions. The editor allows you to cut, copy, paste, move, and search or replace sections of code as needed. Shortcut keystroke combinations are also available for all operations for fast keyboard access to these functions.

Four interactive window areas allow for development and testing of programs you have created. Any two of these windows may be displayed at one time.

- *The Program Window* has a full screen editor for program development and execution.
- *The Interactive Window* is a scratch pad area specifically designed for execution of designated sections of program code.
- *The Standard Input/Output Window* allows you to view data that has been computed or collected by the program as well as input data requested by an executing program.
- *The Error List Window* displays syntax and execution errors found in an executing program.

In the Interactive Mode, your programs execute interpretively allowing you to set breakpoints as well as run the program in a step mode for debugging purposes. The run-time debugger is very flexible and allows for source code level tracing, highlighting of selected portions of code, and code exclusion from compilation. Program variables and data may be viewed and modified on the fly when executing a program under full screen variable and array display options.

Automatic Code Generation

LabWindows 2.0 is designed around a unique interface called a function panel. This function panel gives access to the entire range of LabWindows libraries. The function panel is an intuitive, full screen interface allowing library function execution without the tedious process of entering and editing program code. All parameters for the library functions are represented by pictorial controls directly on the function panel.

Parameters are selected and entered using these pictorial controls. Functions may be immediately executed by selecting the GO command from the command list at the top of the panel. Functions from the instrument library, for example, may be executed immediately thus verifying instrument response in much the same way that functions from the graphics library may be executed interactively for screen layout without manually writing and editing the required code.

This speeds data capture, analysis, and display time, allowing you to concentrate on the task at hand rather than waiting weeks or even months to set up your application, write the code and finally see the displayed data.

Program code required to perform a specific library function is automatically generated at the bottom of the function panel as the pictorial controls are accessed and manipulated. This code can then be executed, modified, or copied directly into your program by selecting the KEEP command from the command list.

LabWindows 2.0 Support

LabWindows has two libraries for instrument control functions. One is for full talker, listener and controller support for IEEE-488 (GPIB)-based instrumentation and the other for RS-232 based instruments. The GPIB library includes many IEEE-488 functions including read, write, clear, trigger, status, serial poll, wait for SRQ, and much more.

The incorporated driver supports both the AT-GPIB board for PC/AT machines and the GPIB-II/IIA for PC/XT machines. Both these drivers are powerful and flexible enough to support all GPIB and RS-232 instruments. LabWindows 2.0 allows data transfer from the external GPIB-based instrument to your computer memory for immediate graphic display or mathematic manipulation or to disk files for data logging applications.

The RS-232 library includes functions for performing input and output over multiple RS-232 (including those from DATEL's MCOMM-232 and MCOMM-422 boards) serial ports under interrupt control, including read, read byte, read terminated buffer, write, write byte, read to file, write from file, manage input/output queue, configure port, get port status, set XON/XOFF modes, send break, and set CTS mode.

In addition to the AT-GPIB and GPIB-II/IIA boards, LabWindows supports the PC-DIO-24, PC-DIO-96 (digital I/O cards), and the PC-TIO-10 (counter/timer board) for the PC/XT bus. With the functions in the Data Acquisition Library, all of these boards may be programmed from the function panel by simply selecting the appropriate pictorial controls.

LabWindows GPIB, RS-232 and the Data Acquisition Libraries may be used separately or in conjunction with any of your other programs. Because the library modules are so flexible, programs may be developed that combine the functions of various libraries for creation of "virtual" instrumentation, or each module may be used in a stand-alone mode of operation.

LabWindows Instrument Library

The *Instrument Library* has over 50 ready-to-use modules for a wide variety of instruments. Each module is complete and allows immediate communication and data processing from the instrument. Also included are a multitude of modules for communicating with many common GPIB-based instruments.

For example, the function "read.waveform(1, wave)" might access a GPIB-based oscilloscope for a captured waveform on channel 1, read the raw data, convert this data to real numbers, and place the data in an array named "wave". Low level GPIB command syntax and associated overhead is reduced to a single command line that is written for you. Complete TLC capability is achieved with a single module.

Operation is fully transparent so that data may be collected immediately. Since the supplied modules were developed using standard LabWindows tools, you can create your own custom modules for data capture and analysis. This user-extensible feature allows you to create custom modules using a special screen oriented editor resulting in your own function panel user interface.

Once this has been created, you simply write the underlying control code in QuickBASIC or C. The resultant module is then stored in a file that can be either QuickBASIC or C oriented regardless of the language used to develop the function.

LabWindows Graphics Library

The *Graphics Library* is a very flexible set of functions designed specifically for data presentation on both screen and hardcopy. Two-dimensional color plots for line, connected point, scatter, and bar charts are available as is real-time graphics (strip charts, numeric plots), linear, log, and semi-log plots.

Single and multiple curve plots are standard with support for both integer and floating point data types are supported. Labeling, scaling, grid type, point style, and color are user selectable. Graphs may be stored and retrieved from disk once created. Multiple, independent viewports may be created with individually defined display attributes.

For example, the plots or waveforms displayed in one viewport may be changed or manipulated without affecting any other port on the screen. Multiple curve fits, connected point plots, scatter charts, and/or bar charts may be created and displayed. Hardcopies may be obtained by dumping the screen to dot-matrix printers, high resolution laser printers, or to GPIB/RS-232 compatible plotters.

LabWindows Formatting and I/O Library

Several useful modules for converting data from ASCII (string variables), used by serial and GPIB-based instruments, to numeric format are included as are conversion routines for integer array to real array, screen input/output functions, and file input/output functions. Numeric data may then be passed to the *Analysis and Graphics Libraries* for manipulation. Additionally, special binary data format conversion routines are also included. The *Formatting and I/O Library* also has functions for creating and reading ASCII and binary files in user-defined formats.

LabWindows Standard Analysis Library

The *LabWindows Standard Analysis Library* contains modules for array and matrix manipulation, complex mathematics such as logarithmic, exponential, and trigometric functions as well as powerful statistical functions. One and two dimensional array addition, subtraction, multiplication, division, inversion, linear evaluation, and min/max values are supported. Sub-arrays may be defined and manipulated.

Full support for scalar/1-dimensional complex mathematics and rectangular-to-polar, polar-to-rectangular conversions are standard functions. Machines equipped with a math coprocessor will see enhanced speed and accuracy. If the coprocessor is not installed, LabWindows uses emulation routines for floating point calculations.

LabWindows Advanced Analysis Library

In addition to the standard LabWindows Libraries outlined above, an *Advanced Analysis Library* is available. This *Advanced Analysis Library* extends the capability of the *Standard Analysis Library* by adding many powerful analytical and processing functions.

In addition to the *Standard Analysis Library*, the *Advanced Analysis Library* contains functions for Fast Fourier (FFT) and Fast Hartley (FHT) Transforms, numeric integration and differentiation, power spectrum analysis, correlation analysis, digital filters (Butterworth & Chebyshev), RMS calculations, linear equation problem solving capability, polynomial and exponential curve fit, and enhanced statistical functions.

As with all LabWindows Libraries, all functions may be integrated into your application program or may be used in the standalone mode for discrete analysis. Mathematical coprocessor will be implemented, if installed.

Hardware Requirements

A minimum system compatible with LabWindows is an IBM-PC/XT/AT (or compatible) or PS/2, a graphics adapter card, MS-DOS operating system, 640K of RAM memory, one hard disk drive, one floppy disk drive. In addition, the following optional equipment may be necessary depending upon application; GPIB interface card (GPIB-II/IIA or AT-GPIB), one or more serial ports, and any digital I/O and counter timer cards (PC-DIO-24/96 & PC-TIO-10), a dot matrix or laser printer or compatible plotter.

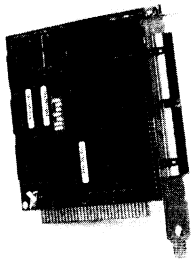
LabWindows supports over 150 dot matrix and laser printers including; HP LaserJet/ThinkJet, Epson FX/LQ series, IBM Proprinter, and any HP-GL compatible plotter. LabWindows also supports most popular graphics cards.

ORDERING INFORMATION

LabWindows 2.0/5	5 1/4" Diskette
LabWindows 2.0/3	3 1/2" Diskette
LabWindows 2.0/5AA	5 1/4" Diskette w/advanced Analysis Library
LabWindows 2.0/3AA	3 1/2" Diskette w/advanced Analysis Library

PC-TIO-10
10 Channel Counter/Timer Board for IBM-PC/XT/AT

FEATURES



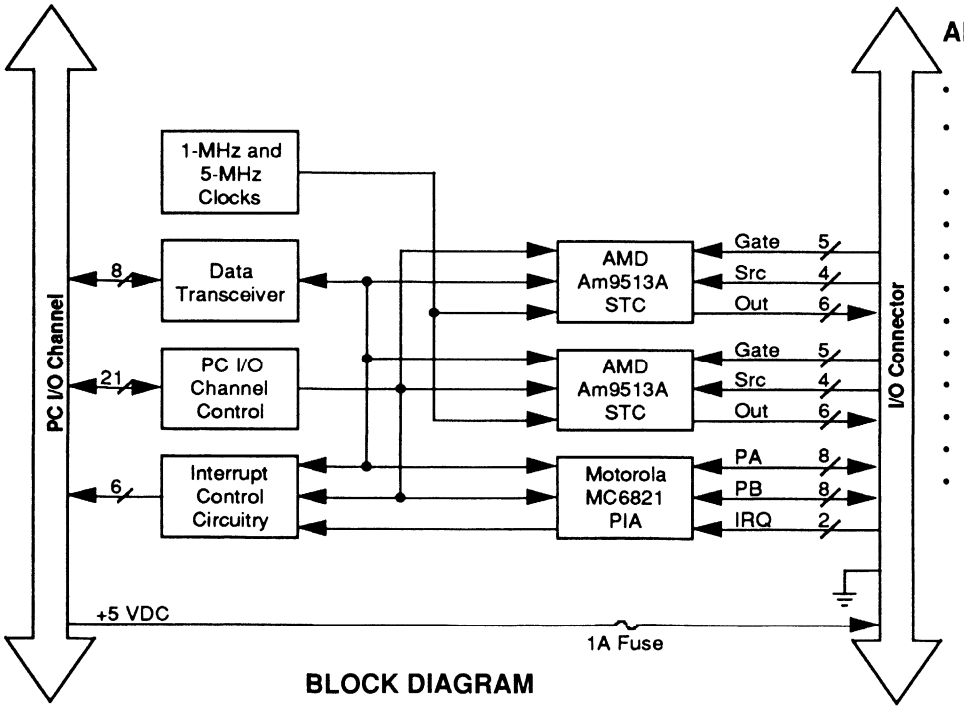
- **10 parallel (TTL Level) 16-bit counter/timers**
- **16 parallel digital I/O lines (bidirectional)**
- **2 external interrupt lines**
- **Counter/Timer rates to 5 MHz**
- **100% compatible with LabWindows Software Package**
- **Delivery from stock! Very low cost!**

GENERAL DESCRIPTION

DATEL's PC-TIO-10 is a very high performance, low cost 10 channel Counter/Timer board designed for IBM-PC/XT/AT and compatible personal computers. Each of the 10 input channels are a full 16-bits wide with update speeds to 5 MHz (200 nSec resolution). Additionally, the PC-TIO-10 has 16 bidirectional, parallel digital I/O lines. Designed around two AMD Am9513A System Timing Controller (STC) chips and one MC6821 PIA (Digital I/O), the PC-TIO-10 allows PC/XT/AT interface to a wide variety of applications including waveform synthesis and generation, event counting, pulse generation, frequency counting to 5 MHz, control sequencing, coincidence alarming, period measurements, programmable one-shot or continuous outputs, up/down counting, periodicity analysis, totalizing, and much more. Each Am9513A (5 channels) may be cascaded for a single channel counter or timer of up to 80-bits. The half size board is bus compatible with both the IBM-PC/XT and IBM-PC/AT and provides for periodic interrupt capability via one of six interrupt lines (jumper selectable). The base address of the PC-TIO-10 is set via a single 7-gang DIP switch on the board.

The 16 digital I/O lines may be used for applications such as external control of power supplies and solid state relays as well as simple, byte-wide data I/O and other discrete monitoring and control applications often found in industry and research laboratories. Additionally, port A is configured as a low drive CMOS compatible output while port B is a high drive, totem-pole configuration capable of TTL compatible outputs suitable for SSR and Darlington-type switch control applications.

All channel control circuitry including channels latches, address decoding, data buffers, and interface timing and control are built into the PC-TIO-10 so that you need not be concerned with writing complex control software. However, it's flexible design allows the experienced programmer direct access to many of the functions of each Am9513A STC chip for direct manipulation/control. DATEL also provides a low cost library of functions for programming the PC-TIO-10 from Microsoft C or QuickBASIC. Additionally, we provide several simple



BLOCK DIAGRAM

APPLICATIONS

- **Waveform Synthesis**
- **One-shot and Continuous Pulse Outputs**
- **Event Counting**
- **Frequency Counting**
- **Control Sequencing**
- **Coincidence Alarming**
- **Period Measurements**
- **Up/Down Totalizing**
- **Binary/BCD Counting**
- **Time-of-Day Clocking**
- **Waveform Analysis**
- **Waveform Generation**

example programs in the User's Manual allowing even the novice programmer immediate access to the PC-TIO-10. National Instruments LabWindows 2.0 may also be used with the PC-TIO-10. A 50-pin header brings all input and output control pins for each counter, 2 interrupt request lines, and +5V dc and GND out to the rear of the IBM PC/XT/AT. An optional, removable ribbon cable and screw terminal connector block is available for signal I/O connections.

HARDWARE CAPABILITY

Am9513A System Timing Controller (STC)

Two STC's are used on each PC-TIO-10, each of which has 5 x 16-bit Counter/Timer channels. The channels may be cascaded to form two channels of 80-bit counter/timers. These STC`s operate in a wide variety of different modes. Each device has a gate, source and output for the 5 x 16-bit counters as well as an independently controlled frequency scaler output for pulse output timing. The main frequency input is connected to a 1 MHz clock allowing count resolutions to 1 µSec. Each counter gate and output is routed to the 50-pin output header. However, only 8 of the counter sources are brought out with the source of counter 5 (from each device) tied to a 5 MHz clock for 200 nSec resolution.

MC6821 Peripheral Interface Adapter (PIA)

Each PC-TIO-10 contains a single MC6821 PIA capable of bidirectional data I/O from 2 x 8-bit ports with associated control lines. The individual I/O lines of the 2 x 8-bit ports may be programmed as inputs or outputs and changed at any time. While the two ports are programmed similarly, they are unique in that port A is a low-drive CMOS compatible output while port B is a high drive TTL compatible output suitable for Darlington switch control applications.

Data Transceiver

The data transceiver buffers all data between the PC-TIO-10 and the IBM PC/XT/AT I/O channel. All data transfers are byte wide (8-bits).

I/O Channel Control

Operational control of the PC-TIO-10 is regulated by the I/O channel control circuitry in conjunction with bus control signals. These bus control signals regulate the type of bus cycle in progress.

Additionally, the I/O channel control circuitry monitors PC/XT/AT address lines for specific PC-TIO-10 address selection. The base address of the PC-TIO-10 is set via an 8-gang DIP switch.

Interrupt Control

Interrupt requests are regulated by the interrupt control circuitry via one of two interrupt input lines on the PC-TIO-10. One of six PC/XT/AT interrupt request lines may be selected (jumpers). Interrupt enable bits may be set via software for maximum flexibility.

I/O Connector

All signal I/O is accomplished through a 50-pin male header at the rear of the PC-TIO-10. A 50 conductor ribbon cable and screw termination box are also available (optional). The SOURCEn, GATEn, and OUTn (see connector pinout) are the source, gate, and output signals for the respective STCs. The TIRQ1 and EXTIRQ2 are the interrupt input signals for the PC-TIO-10. The An and Bn pins designate the various bits of port A and B. Power from the PC/XT/AT I/O channel is also available on pin 34.

CONNECTOR PINOUT

SOURCE 1	1	2	GATE 1
OUT 1	3	4	SOURCE 2
GATE 2	5	6	OUT 2
SOURCE 3	7	8	GATE 3
OUT 3	9	10	SOURCE 4
GATE 4	11	12	OUT 4
GATE 5	13	14	OUT 5
SOURCE 6	15	16	GATE 6
OUT 6	17	18	SOURCE 7
GATE 7	19	20	OUT 7
SOURCE 8	21	22	GATE 8
OUT 8	23	24	SOURCE 9
GATE 9	25	26	OUT 9
GATE 10	27	28	OUT 10
FOUT 1	29	30	FOUT 2
EXTIRQ 1	31	32	EXTIRQ 2
GND	33	34	+5V
A0	35	36	A1
A2	37	38	A3
A4	39	40	A5
A6	41	42	A7
B0	43	44	B1
B2	45	46	B3
B4	47	48	B5
B6	49	50	B7

SOFTWARE SUPPORT

DATEL carries a complete line of software support tools for the PC-TIO-10. From a low-cost function (utility routines) library allowing user to write their own application specific routines in Microsoft "C" or QuickBASIC. Additionally, National Instruments LabWindows 2.0 is available from DATEL allowing you to graphically create your own acquisition and control routines without programming (refer to LabWindows documentation for a complete description).

SPECIFICATIONS

(All specifications are typical at 25 °C unless otherwise noted)

INPUT/OUTPUT LIMITS

Counter/Timer I/O
Input Logic (low)
- Minimum 0V
- Maximum 0.8V

Input Logic (high)
- Minimum 2.2V
- Maximum 5.25V

Output Logic (low)
- at 3.2 mA, minimum 0V
- at 3.2 mA, maximum 0.4V

Output Logic (high)
- at -200 µA, minimum 2.4V
- at -200 µA, maximum 5.0V

Input Load Current
- (0 < Vin > 5.25V), minimum ..... -10 µA
- (0 < Vin > 5.25V), maximum ..... 10 µA

DIGITAL I/O LINES

Input Logic (low)
- Minimum 0V
- Maximum 0.8V

Input Logic (high)
- Minimum 2.0V
- Maximum 5.25V

Output Logic (low)
- at 3.2 mA, minimum 0V
- at 3.2 mA, maximum 0.4V

Output Logic (high)
- at -200 µA, minimum 2.4V
- at -200 µA, maximum 5.0V

Port A Input Low
- at 0.4V, maximum ..... -2.4V

Port A Input High
- at 2.4V, maximum ..... -200 µA

Port B Input Leakage
- (0.4V to 2.4V) ..... 10 µA

Port B Darlington Drive
- at 1.5V ..... -1.0 mA to -10.0 mA

TIMING I/O

Channels 10 ..... (5 channels per STC cascadable)
2 Frequency Scaler Outputs
Resolution ..... 16-bits (counters/timers)
4-Bits (Frequency Scaler)
Base Clocks ..... 5 MHz
1 MHz
100 KHz
10 KHz
1 KHz
100 Hz
Clock Accuracy ..... ±0.01%
Signal Compatibility ..... TTL (inputs and outputs)
Source Frequency, maximum ..... 7 MHz
Source Cycle Time, maximum ..... 145 nSec
Source Pulse Duration, minimum ..... 70 nSec
Gate Pulse Duration, minimum 145 nSec

EXTERNAL INTERRUPTS

Channels 2
Sensitivity
(Software Programmable) ..... Rising/Falling Edge
Pulse Width, minimum ..... 100 nSec
Compatibility
(with 4.7 Kohm Pull-up Resistors) ..... TTL

POWER CONSUMPTION

+5V dc
- Typical ..... 0.6 A

PHYSICAL

Dimensions ..... 3.9" x 4.75"
I/O Connector ..... 50-pin, male ribbon cable connector

ENVIRONMENTAL

Operating Temperature ..... 0 °C to +70 °C
Humidity (rH non-condensing) ..... 5% to 90%

PC-DADiSP
Signal Display and Analysis Worksheet Software

FEATURES

- **Accepts analog signal data files; limited only by disk size**
- **Over 300 graphics and math functions**
- **Displays and manages up to 100 windows**
- **Comprehensive DSP/FFT processing**
- **"No-programming" pop-up windows and menus for ease of use**
- **Powerful macros to customize your application**

GENERAL DESCRIPTION

The PC-DADiSP Signal Processing Worksheet™ displays and analyzes the analog signal output files from DATEL's PC-Series fast A/D boards and other analog input boards. PC-DADiSP is a unique software math package offering an interactive graphic environment for A/D signals. The product operates on all PC/AT-compatible 80286, 80386, or 80486 computers equipped with extended memory.

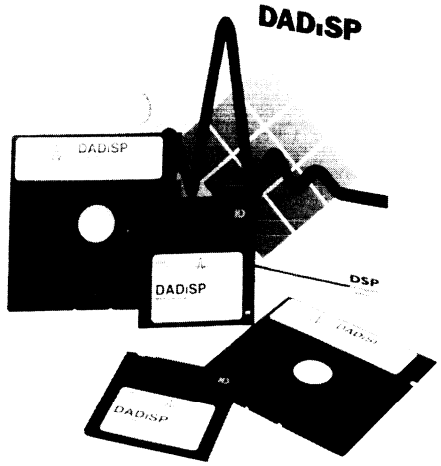
The worksheet functions like a financial spreadsheet but displays data graphically. Convenient pop-up menus can review data for a signal file. Both the raw input A/D data and math-processed output data can be simultaneously displayed in multiple windows. Using simple controls, any portion of the signal file may be zoomed, scaled, panned, or scrolled. Math parameters may be chained between multiple windows and updated together automatically, as in a spreadsheet. No programming is required.

Each window acts as a highly-maneuverable viewport to a larger data set limited only by disk size. Screen images may be printed out on a wide variety of hardcopy devices including laser and dot-matrix printers.

Display formats include bar chart, tabular, line plots, waveform envelope, and 3D surface plots. Over 300 unique functions are included such as peak detection, noise smoothing, histograms, and standard deviation. DSP functions offer a large choice of windowing, FFT display, IIR, and FIR filters.

PC-DADiSP reads integer binary and ASCII floating point data files such as those used with Lotus 1-2-3™ formats. Parameters such as trigger rates, operator name, date and location, conversion formulas, unit names, and data source may be saved in a Worksheet template. In addition, PC-DADiSP may be customized and extended using a powerful interactive macro language.

Examples of PC-DADiSP power include fast-rolloff filtering, notch-filter removal of carrier beat frequencies, 3D display, and cross-channel computation for heat flow studies. All menus are in plain English and have a logical, intuitive feel for how the analysis would proceed. Waveforms may be annotated and signal portions can be extracted and connected to other signals. PC-DADiSP accepts data from A/D sources in 2- to 32-bits.



PC-DADiSP is compatible with the PC-414, -411, -412, -430, and other DATEL A/D boards. The system includes a comprehensive user's manual and is compatible to all popular display adapters including EGA, VGA, and Hercules™.

SYSTEM REQUIREMENTS

- 2 Megabytes of extended memory (i.e. 2.5 Mb of total memory) or greater up to 16 Mb.
- MS-DOS 3.0 or higher.
- VGA, EGA, CGA, or Hercules display adapter.

FUNCTIONS

Series and scalar math
Fourier transform and related functions
  Includes several window types, auto-correlation, convolution and more
Trigonometric functions
Statistical functions:
  Integrals, derivatives, standard deviation, error, etc.
Peak analysis
Generated series including Hamming, Hanning, and Kaiser FFT windows
Series display, XY functions, processing and manipulation
Data conversion, extraction and window control
DSP pipeline - macros
Coordinate manipulation
String functions, control flow, annotation, query functions
Menu, macro, and command file functions
Hardcopy, plotting (including laser printers)
Digital Filtering

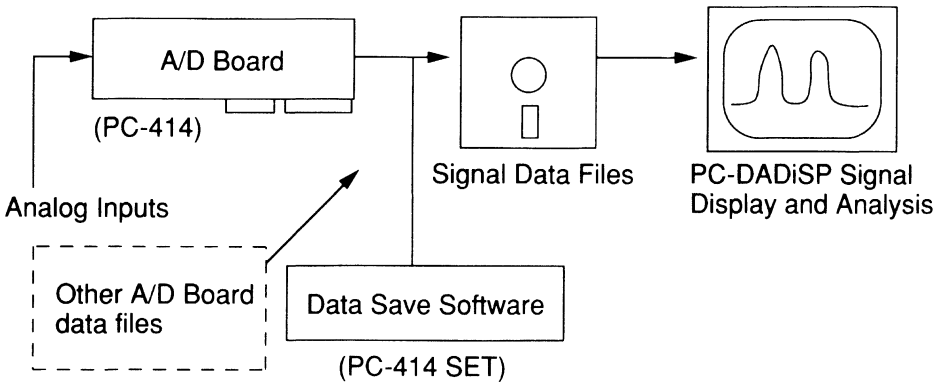


Figure 1. Configuration Diagram

APPLICATIONS

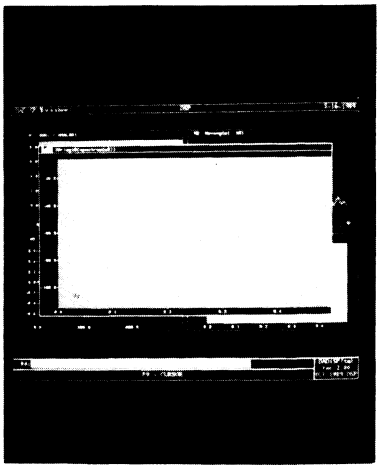


Figure 2. Filtering

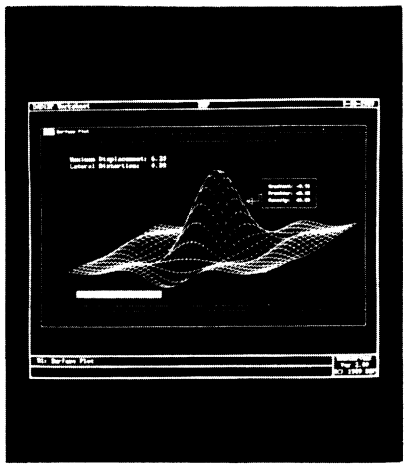


Figure 3. 3D Plotting

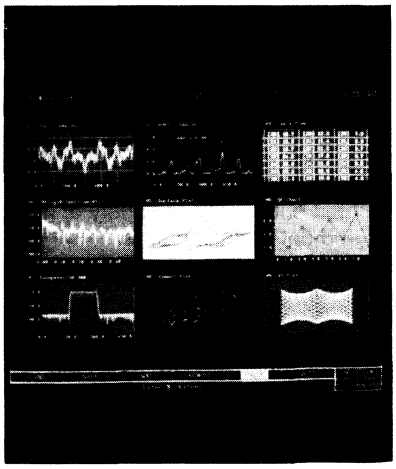


Figure 4. Multiple Windows

ORDERING INFORMATION

PC-DADiSP	Signal Display and Analysis Worksheet Software

Includes 3.5-inch and 5.25-inch disks, parallel port access key, and manuals.

Contact DATEL for:

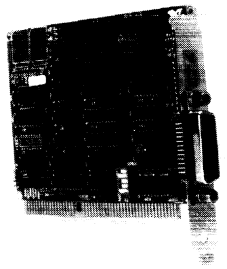
- **Data Acquisition & Control Boards**
- **Panel Meters, Printers, & Calibrators**
- **Data Conversion Components**
- **Power Supplies**

Dial
1-800-233-2765
for
Immediate Assistance

AT-GPIB
High Speed Instrumentation Interface Board for IBM-PC/AT

FEATURES

- **Full IEEE-488.2 (GPIB) compatibility**
- **Uses National Instruments NAT4882 and TURBO488 ASICs**
- **Data transfer speeds to 1 megabyte/sec**
- **FIFO Buffers for complete GPIB to PC/AT bus decoupling**
- **Choice of 11 interrupt lines**
- **Choice of three 16-bit DMA channels**
- **Full 16-bit GPIB to PC/AT bus transfers**
- **FREE Software for complete Talker/Listener/Controller Support**

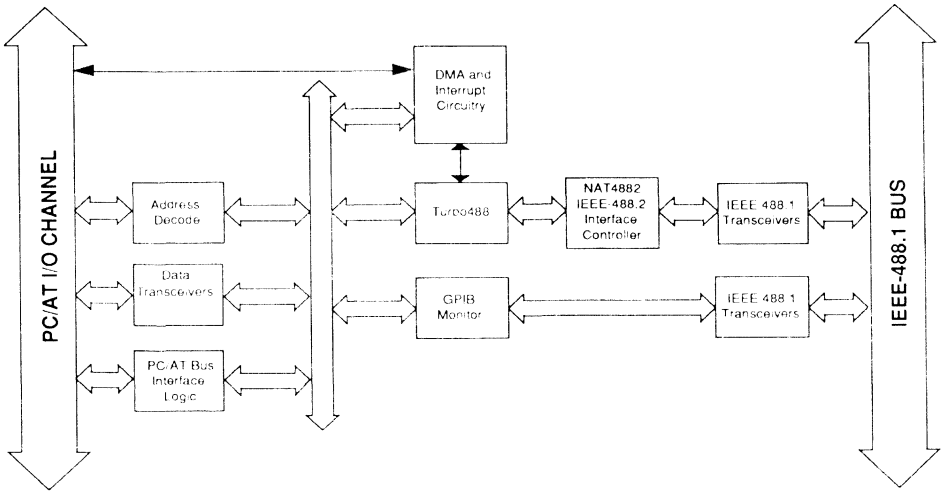


GENERAL DESCRIPTION

DATEL's AT-GPIB is the high performance IEEE-488.2 champion! It's low cost, full Talker/Listener/Controller support, and very high speed (1 megabyte/sec transfers speed) coupled with FREE software support means virtually anyone can be up and running in minutes. Designed around National Instrument's NAT4882 and Turbo488 ASICs (Application Specific Integrated Circuit), the AT-GPIB is a full function instrumentation interface card conforming to all revisions of the IEEE-488 standard including IEEE 488.2-1987. Full handshake and interface management functions are built directly on the board. On-board monitor and diagnostic circuitry adds flexibility to the AT-GPIB for applications such as testing proper low-level functionality of GPIB compatible instruments.

Used specifically for interfacing IBM-PC/AT personal computers (and compatibles) to the vast array of programmable devices via the General Purpose Interface Bus (often called HP-IB), the AT-GPIB takes full advantage of the PC/AT's 16-bit parallel architecture for extremely high speed data transfers. The emerging popularity of the PC/AT bus for instrumentation interface means you can upgrade now without the worry of obsolescence.

The NAT4882 interface controller performs the basic IEEE-488 Talker/Listener/Controller functions as well as the enhanced Controller functions required by the most recent revision of the IEEE-488 standard. The interface controller is accessed



BLOCK DIAGRAM

APPLICATIONS

- **Controller for up to thirteen Benchtop Instruments**
- **Interface to Wide Variety of Scopes, DMM's, Analyzers**
- **Very High Speed Data Collection**
- **Data Communication Between Local Controller and Remote Instruments**
- **Engineering/Test Bench Data Concentrator**
- **Production/Manufacturing Automation**

through the Turbo488 and contains program registers for configuration, control, and monitoring of AT-GPIB IEEE-488 interface functions as well as transferring commands and data to and from other IEEE-488 devices. Operating at a clock speed of 20 MHz, the NAT4882 is the fastest GPIB chip available. It is also software compatible with the NEC uPD7210 and TI 9914A.

The Turbo488 ASIC is a high speed CMOS device that allows sustained data transfers at the maximum specified rate of 1 megabyte/sec for both reads and writes. The Turbo488 increases the performance of data I/O transfers via software (programmed) as well as data transfer via the high speed DMA controller on the PC/AT motherboard. The Turbo488 contains FIFO buffers allowing complete GPIB to PC/AT bus transfer decoupling as well as allowing a 16-bit PC/AT bus interface with byte-to-word packing and unpacking in hardware. The use of these two ASICs significantly increases throughput associated with GPIB driver software. Standard IEEE-488 cables may be used to connect the AT-GPIB with up to thirteen instruments (the on-board diagnostics take up one additional bus load).

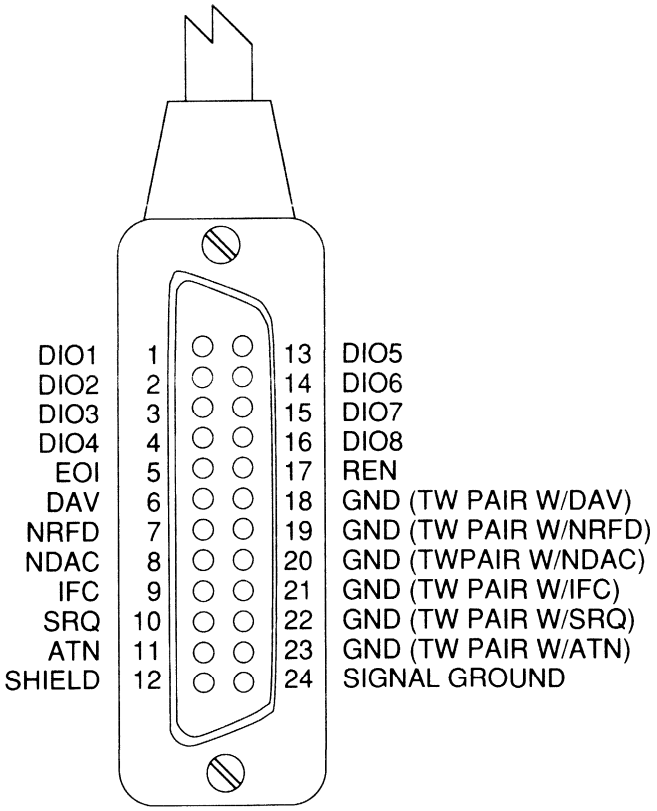
Each AT-GPIB board is supplied with a full set of FREE software drivers including an interactive configuration program, an interactive control program, and diagnostics that are fully compatible with MS-DOS. This package is installed as part of the operating systems and may be accessed from all popular languages including BASICA, Professional BASIC, Microsoft C, and QuickBASIC. Also, a Universal Language Interface (ULI) is included allowing use of standard I/O functions such as BASIC PRINT and INPUT statements to send/receive HP-style commands to and from the driver from most DOS languages and spreadsheets. The AT-GPIB is fully compatible with LabWindows 2.0 (optional) for full menu-driven operation.

IEEE-488.1 and .2 (GPIB) COMPATIBILITY

The General Purpose Interface Bus (GPIB) is defined by ANSI/IEEE Standard 488.1-1987 and is often referred to as the IEEE-488 bus (also called HP-IB). It's high speed and very well defined protocol make it extremely popular (and growing) for interfacing programmable devices with computers. The AT-GPIB is compatible with all revision levels of the IEEE-488 standard including IEEE-488.2-1987. The IEEE-488 standard specifies allowable subsets of interface functions. The codes supported by the AT-GPIB are listed in the following table:

CAPABILITY CODE	DESCRIPTION
SH1	Source Handshake
AH1	Acceptor Handshake
T5, TE5	Talker, Extneded Talker
L3, LE3	Listener, Extended Listener
SR1	Service Request
PP1, PP2	Local/Remote Parallel Poll
RL1	Remote/Local
C1, C2, C3, C4, C5	Controller
E1, E2	Three-state bus drivers with automatic switch to open collector, during Parellel Poll

CONNECTOR PINOUT



Talker

The AT-GPIB has all the Talker requirements for an IEEE-488.2 Controller: basic Talker with unaddress if MLA (T5, TE5) as well as supporting optional functionality: respond to a Serial Poll and a Talk-only mode.

Listener

The AT-GPIB has all the IEEE-488.2 Listener requirements for receiving device-specific messages: basic Listener with unaddress if MTA (L3, LE3) as well as optional Listen-only capability.

Controller

The AT-GPIB has all required IEEE-488.2 Controller function capabilities: System Controller (C1), send IFC and take charge (C2), send REN (C3), respond to SRQ (C4), send interface messages (C5), and take control synchronously (C5). Also implemented are optional functions: receive control (C5), pass control (C5), pass control to self (C5), and parallel poll (C5).

Passing Control

The AT-GPIB can pass and receive control and implements the following required functions: C1, C2, C3, C4, C5, T5, TE5.

Electrical

The AT-GPIB implements the IEEE-488 required E2 electrical interface. Open-collector drivers drive the SRQ, NTFD, and NDAC signal lines. Tri-state drivers drive the DAV, EOI, ATN, REN, and IFC signal lines. When an IEEE-488 device in a IEEE-488 system is not in Parallel Poll Active State (PPAS), the AT-GPIB uses three-state drivers to drive the DIO1 through 8 signal lines. If an IEEE-488 device in the IEEE-488 system is in Parallel Poll Active State (PPAS), the AT-GPIB uses open-collector drivers to drive the DIO1 through 8 signal lines.

ADDITIONAL REQUIREMENTS

The AT-GPIB implements all of the additional IEEE-488.2 requirements including:

- Provide low-level GPIB control for:
  - Pulse IFC TRUE for greater than 100 µSec
  - Set the REN signal line either TRUE or FALSE
  - Send any interface message (singly or combination) defined in IEEE-488
  - Send and detect IEEE-488 END message
- Input and Output all IEEE-488.2 codes, formats, protocols, and commands
- Sense the state of SRQ signal line
- Sense TRUE to FALSE SRQ line transitions
- Examine the status byte on a bit by bit basis
- Detect error conditions of the AT-GPIB attempting to source handshake a byte while all other devices are in AIDS
- Timeout on AT-GPIB-to-device and device-to-AT-GPIB message exchanges

RECOMMENDATIONS

The AT-GPIB implements all IEEE-488.2 Controller recommendations including:

- Monitor bus lines - PC/AT monitoring of all bus lines via AT-GPIB circuitry
- Timeouts - Timeout values can be varied via AT-GPIB
- SRQ Interrupts - AT-GPIB interrupt request upon SRQ transition (0 to 1)

HARDWARE CAPABILITY

Address Decode

The AT-GPIB occupies 32 bytes in the I/O address space of the PC/AT. The base address is set via a 5-gang DIP switch. Decoding is accomplished by matching the address lines on the AT-GPIB to those on the PC/AT I/O channel and enabling reads and writes to the GPIB interface controller (NAT4882) via the Turbo488.

Data Transceivers

The AT-GPIB uses the full 16-bit data path of the PC/AT I/O bus. The number of accesses to the AT-GPIB by the controller is effectively halved, thereby substantially increasing data throughput.

PC/AT Bus Interface Logic

The AT-GPIB buffers all signals to and from the PC/AT bus to ensure that electrical noise does not affect reliability.

DMA and Interrupt Logic

The AT-GPIB requests interrupts from the CPU via one of 11 jumper selectable interrupt request lines. Interrupt request lines 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15 may be selected. Full 16-bit Direct Memory Access (DMA) can be accomplished on DMA channels 5, 6, or 7 (jumper selectable). The AT-GPIB uses PC/AT DMA controller demand-mode transfers vs normal cycle-steal transfers. This allows the maximum IEEE-488 bus specified performance of 1 megabytes/sec.

SOFTWARE SUPPORT

Each AT-GPIB is supplied with a FREE software package (NI-488.2 MS-DOS) which includes an MS-DOS handler that has all GPIB Talker/Listener/Controller functions and installs as part of the operating system. This handler may be accessed via all popular languages such as BASICA, Microsoft C, and QuickBASIC.

Besides the free software, the AT-GPIB is supported by LabWindows 2.0 (refer to LabWindows documentation for a complete description).

SPECIFICATIONS

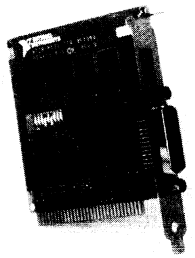
(All specifications are typical at 25 °C unless otherwise noted)

CLOCK INPUTS	
Turbo488 Clock	20 MHz
NAT4882 Clock	20 MHz
IEEE-488 BUS TRANSFER RATES	
Read from GPIB Instrument	
Maximum	1 Megabyte/sec
Write to GPIB Instrument,	
Maximum	1 Megabyte/sec
GPIB Commands, maximum	350 Kbytes/sec
(Actual rates are instrumentation dependant)	
POWER REQUIREMENTS	
+ 5 V dc	
Typical	0.66 A
Maximum	1.50 A
PHYSICAL	
Dimensions	4.2" x 6.5"
I/O Connector	IEEE-488 standard 24-pin
Operating Temperature	0 °C to +70 °C
Humidity (non-condensing)	5% to 90%
Storage Temperature	-55 °C to +150 °C

GPIB-PCIIA
High Speed Instrumentation Interface Board for IBM-PC/XT/AT and PS/2

FEATURES

- **Full Function Talker/Listener/Controller (TLC)**
- **Half size board fits any bus I/O slot**
- **Interface up to 15 instruments per interface card**
- **Shared interrupt capability for IBM GPIB adapter compatibility**
- **Fully compatible with LabWindows 2.0 Software**
- **Data transfer rates to 300 Kbytes/sec**
- **Transparent DMA handling**
- **FREE software package**

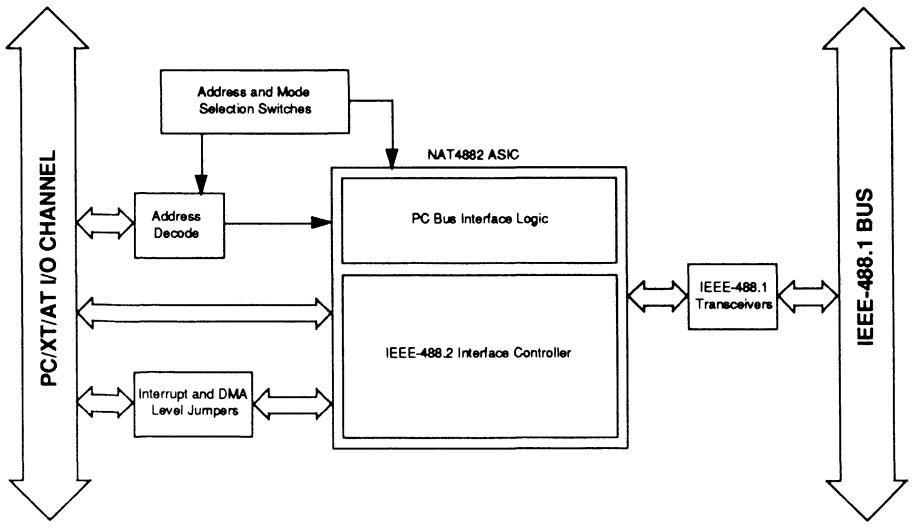


GENERAL DESCRIPTION

DATEL's GPIB-PCIIA is a low cost, full function instrumentation interface card (half-size) conforming to the ANSI/IEEE 488-1978 standard. This high speed, 8-bit parallel bus is extremely popular and has long been the method of choice for importing data from benchtop instruments, controlling and setting up instruments, and for interconnecting a wide variety of compatible instruments to a single Talker/Listener/Controller ...the personal computer. The GPIB-PCIIA is supplied with a FREE software package that eliminates the need for intimate knowledge of the hardware or understand the IEEE-488 protocol.

Used specifically for interfacing IBM-PC/XT/AT and PS/2 personal computers (and compatibles) to the vast array of programmable devices via the General Purpose Interface Bus (often called HP-IB), the GPIB-PCIIA is compatible with all revision levels of the IEEE-488 standard. Full handshake and interface management functions are built directly on the board. Combining National Semiconductor 75160A and 75162A transceivers with NEC uPD7210 GPIB TLC integrated circuit makes the GPIB-PCIIA interface card one of the most versatile instrumentation interfaces available. Standard IEEE-488 cables may be used to connect the GPIB-PCIIA with up to 14 instruments.

Each GPIB-PCIIA board is supplied with a full set of FREE software drivers including an interactive menu-driven configuration program, an interactive control program, and diagnostics that are fully compatible with MS-DOS. This package is installed as part of the operating systems and may be accessed from all popular languages including BASICA, Microsoft C, and QuickBASIC. In addition, the GPIB-PCIIA is fully compatible with LabWindows 2.0 (optional) for full menu-driven operation.



BLOCK DIAGRAM

APPLICATIONS

- **Controller for up to fourteen Benchtop Instruments**
- **Interface for Wide Variety of Scopes, DMM's, Analyzers**
- **High Speed Data Collection via Standalone Instruments**
- **Data Communication Between and Remote Instruments**
- **Engineering/Test Bench Data Concentrator**
- **Production/Manufacturing Automation**

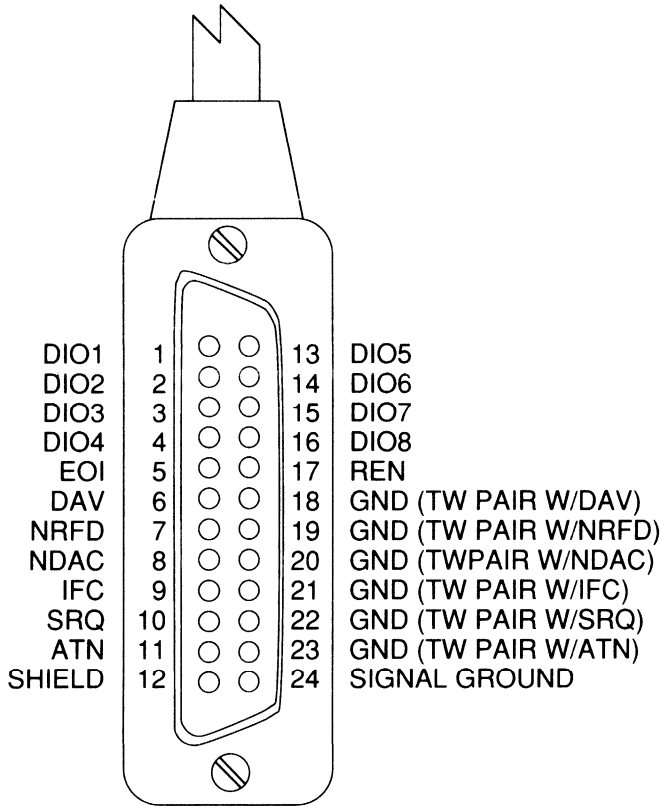
IEEE-488 (GPIB) COMPATIBILITY

The General Purpose Interface Bus (GPIB) is defined by ANSI/IEEE Standard 488-1978 and is often referred to as the IEEE-488 bus (also called HP-IB). The GPIB is an 8-bit parallel digital bus with full handshake and interface management capability. It's high speed and very well defined protocol make it extremely popular (and growing) for interfacing programmable devices with computers. The GPIB-PCIIA is compatible with all revision levels of the IEEE-488 standard.

The IEEE-488 standard specifies allowable subsets of interface functions. The codes supported by the GPIB-PCIIA are listed in the following table:

CAPABILITY CODE	DESCRIPTION
SH1	Source Handshake
AH1	Acceptor Handshake
T5, TE5	Talker, Extneded Talker
L3, LE3	Listener, Extended Listener
SR1	Service Request
PP1, PP2	Local/Remote Parallel Poll
RL1	Remote/Local
C1, C2, C3, C4, C5	Controller
E1, E2	Three-state bus drivers with automatic switch to open collector, during Parellel Poll

CONNECTOR PINOUT



HARDWARE CAPABILITY

Address Decoding

Address Decoding is accomplished by matching the address lines on the GPIB-PCIIA to those on the IBM PC I/O channel and enabling reads and writes to the GPIB interface controller.

Buffering and Data Routing

A bidirectional internal bus handles data transfers between the IBM PC I/O channel and the GPIB interface controller.

Interrupt Arbitration

Interrupt requests may be generated by the GPIB-PCIIA for transparent interrupt handling under control of Interrupt Arbitration circuitry. A choice of six interrupt lines (levels) are available via jumper plugs on the board.

DMA Arbitration

The DMA arbitration circuit recognizes when DMA operations are enabled or disabled and when the last transfer has taken place. It also routes the DMA request and acknowledge signals to the selected DMA channel. A choice of three DMA channels are available using the host DMA controller. All DMA handling is transparent once configured.

Configuration Switches and Jumpers

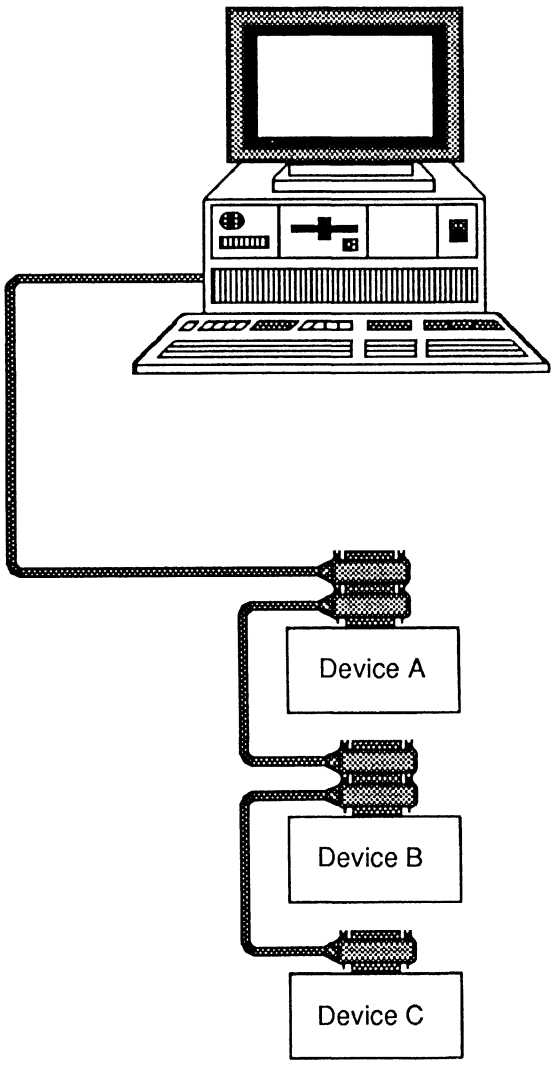
The GPIB-PCIIA contains a 5-gang DIP switch for address channel selection as well as jumpers for interrupt request lines and DMA channel selection.

GPIB Interface Controller

The GPIB-PCIIA employs an NEC uPD7210 which implements virtually all IEEE-488 functions. Twenty-one program registers are to configure, control, and monitor the interface functions as well as to pass commands and data to and from the computer and the GPIB-PCIIA.

GPIB Transceivers

National Semiconductor 75160A and 75162A transceivers are used to interface the Interface Controller (NEC uPD7210) to the IEEE-488 bus. The ICs are specifically designed to provide (glitch-free) power-up/power-down bus protection. Each GPIB-PCIIA counts as a single IEEE-488 bus load and, therefore, up to 14 additional devices may be connected to the bus before exceeding the loading restrictions.



LINEAR CONFIGURATION

SOFTWARE SUPPORT

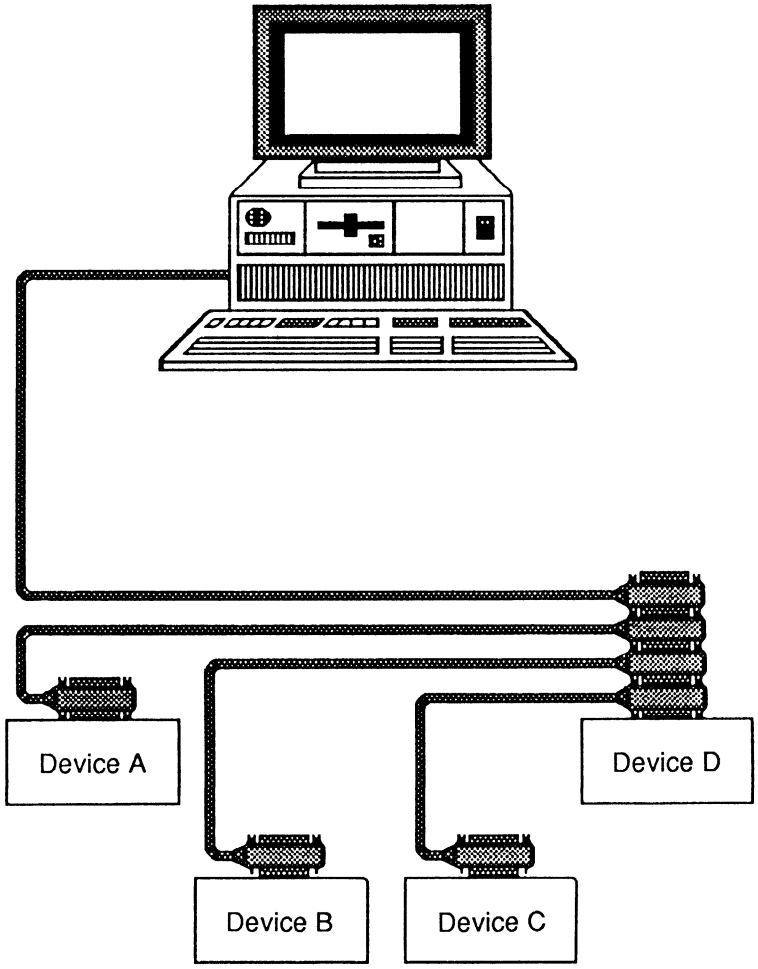
Each GPIB-PCIIA is supplied with a FREE software package (NI-488.2 MS-DOS) which includes an MS-DOS handler that has all GPIB Talker/Listener/Controller functions and installs as part of the operating system. This handler may be accessed via all popular languages such as BASICA, Microsoft C, and QuickBASIC.

Besides the free software, the GPIB-PCIIA is supported by LabWindows 2.0 (refer to LabWindows documentation for a complete description).

SPECIFICATIONS

(All specifications are typical at 25 °C unless otherwise noted)

IEEE-488 BUS TRANSFER RATES	
DMA	> 300 Kbytes/sec
Block Length	up to 64 Kbytes
POWER REQUIREMENTS	
+ 5 V dc	
Typical	0.6 A
Maximum	1.1 A
PHYSICAL	
Dimensions	4.2" x 4.5"
I/O Connector	IEEE-488 Standard 24-pin
Operating Temperature	0 °C to +50 °C
Humidity (non-condensing)	10% to 85%
Storage Temperature	-55 °C to +150 °C



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- **Panel Meters, Printers, & Calibrators**
- **Data Conversion Components**
- **Power Supplies**

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1-800-233-2765
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Data Acquisition Boards for VME Bus

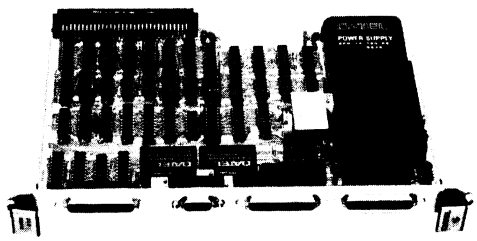
VMEBUS A/D - D/A BOARDS

Model	A/D Channels	A/D Resolution	A/D Speed	Prog. Gain Amplifier	In/Out Ranges	D/A Channels	D/A Resolution	Notes
DVME-601A	16 S/ 8 D Expandable to 256	12 Bits	20 µs	x1 to x1K	5, 10V down to 50 mV	None	---	68010 CPU 256K memory RS-232, 5 TTL I/O Counter/Timers "No prgmg" Command Exec. Vectored interrupt
DVME-601B		12 Bits	4 µs					
DVME-601C		16 Bits	35 µs					
DVME-601D		16 Bits	400 ms					
DVME-601E		12 Bits	2 µs					
DVME-611/612A	32 S / 16 D Expandable to 256	12 Bits	20 µs	x1 to x128 Software Pgmble	5V, 10V down to 50 mV	2 (612)	12 Bits	Short I/O SA:16, SD:16 Vectored interrupt
DVME-611/612B		12 Bits	4 µs					
DVME-611/612C		16 Bits	35 µs					
DVME-611/612D		16 Bits	400 ms					
DVME-611/612E		12 Bits	2 µs					
DVME-611/612F		14 Bits	4 µs					
DVME-613	16 S/8 D Isolated 500V	12-14-16 Bits	40 µs	x1 to x100	5V, 10V down to 50 mV	None	---	8 In/8 Out TTL, SA:24, SD:16 Start timer, interrupt
DVME-624	None	---	---	---	2.5 to 10V 4 to 20 mA	4 Isolated	12 Bits	SA:16, SD:16 350V Isolation
DVME-626	None	---	---	---	5V, 10V	6	16 Bits	SA:16, SD:16
DVME-628	None	---	---	---	2.5 to 10V 4 to 20 mA	8	12 Bits	SA:16, SD:16
DVME-641	32 S/16 D	Slave MUX board	6 µs Settling	---	5V, 10V 4 to 20 mA	---	---	Slave input expander to 601, 611, 612
DVME-643	8D Isolated	Slave MUX board	2.5 ms Settling	x50, x100	5V Down to 50 mV	---	---	Slave input expander to 601, 611, 612
DVME-645	16 S/8D	Slave MUX board	6 µs Settling	---	5V, 10V	---	---	Simultaneous Sample/Hold Expander to 601, 611, 612
DVME-614A	4 Simul. S/H	12 Bits	1.5 MHz	x1 or x10	1V, 5V, 10V	1	12 Bits	4K-sample FIFO memory Analog trigger Parallel data port Sample counter/timer Simultaneous sampling Vectored interrupt
DVME-614B	4 S	14 Bits	500 KHz	---	5V, 10V			
DVME-614C	4 S	12 Bits	1 MHz		5V, 10V			
DVME-614D	1 S	12 Bits	4 MHz		1V			
DVME-614E	16 S	12 Bits	400 KHz	x1 to x100	1, 5, 10V, 100mV			
DVME-630A	4 Simul. S/H	12 Bits	1.5 MHz	x1 or x10	1V, 5V, 10V	None	---	Local 32 MHz 320C30 DSP, 512 K Memory, Fast "no prgmg" command Executive, Interrupt DSP library
DVME-630B	4 S	14 Bits	500 KHz	---	5V, 10V			
DVME-630C	4 S	12 Bits	1 MHz		5V, 10V			
DVME-630D	1 S	12 Bits	4 MHz		1V			
DVME-630E	16 S	12 Bits	400 KHz	x1 to x100	1, 5, 10V, 100mV			
DVME-622	None	---	---	---	5V, 10V	16 Simul. Update	12 Bits	3 µs settling per channel
DVME-621	None	---	---	---	5V, 10V @ 100 mA or 160 mA	4 Isolated	12 Bits	Power DAC's, voltage or current mode, active drivers, 500V isolation

DVME-611/612
32S/16D-Channel VME A/D-D/A Boards

FEATURES

- **Two models of VMEbus-based boards**
  DVME-611: 32 single-ended/16 differential A/D channels
  DVME-612: 32 single-ended/16 differential A/D channels and 2 D/A channels
- **Choice of A/D bits/speed**
  12 bits/2, 4, or 20 µSec.
  14 bits/4 µSec.
  16 bits/35 µSec.
- **Four input voltage ranges available: ±10V, ±5V, 0 to +5V, and 0 to +10V dc**
- **Three types of output coding:**
  Bipolar 2's complement
  Bipolar offset binary
  Unipolar straight binary
- **Up to 400 KHz throughput with a *fast throughput mode* for high-speed data transfers (single channel)**
- **On-board interrupt vector register for host system's service routines**
- **80 dB CMRR at gain of 128**



- **Eight-stage programmable gain amplifier (PGA)**
- **±0.05% full-scale range accuracy for D/A channels**
- **Channel expansion boards for up to 256 channels**
  DVME-641: Non-isolated, high-level inputs
  DVME-643: Isolated, thermocouple, RTD, high-level, 4-to-20 mA inputs
  DVME-645: Simultaneous sample/hold inputs
- **Two TTL digital outputs**

GENERAL DESCRIPTION

The DVME-611/612 are DATEL's VMEbus based high-end A/D conversion boards. The A/D boards provide up to 16-bit binary data from up to 32 single-ended or 16 differential analog input channels. DATEL also offers optional expansion boards for up to 256 single-ended or differential analog input channels. The DVME-612 is also equipped with two D/A channels, operable in four output voltage ranges.

The on-board hardware essentially consists of multiplexers, a PGA, an A/D converter, and registers. The PGA is programmable for gains from 1 to 128 in binary increments. Both the DVME-611 and the DVME-612 are available in several models depending upon the A/D converter module used. The A/D converter modules are easily field-replaceable. All models except the DVME-611D and the DVME-612D contain a sample/hold amplifier.

The host-programmable command register controls the A/D conversion process. Depending upon the contents of the command register, an external trigger may also initiate the A/D conversion process. The host system may obtain information pertaining to the A/D conversion and control selections by reading the status register.

The channel and control information from the channel select logic section is brought out to the J4 expansion connector. The control lines include End of Conversion (EOC), End of Scan (EOS), settling time delay, and external trigger signals. These control signals on the expansion connector are also usable with externally multiplexed input channels. The host system selects the start and final channels for the A/D scanning process.

The analog output section on the DVME-612 offers ±1/2 LSB differential non-linearity and operates at ±0.05% of full-scale range accuracy.

Functionally, the analog signal from the input channel is amplified and converted into binary data. The resolution depends on the A/D converter module used. Figure 1 is a functional block diagram of the DVME-611/612 A/D boards. Data from the A/D converter module is coded via jumpers into straight binary, offset binary, or 2's complement coding. The binary A/D data is transferred to the host system through the VMEbus transceivers.

The DVME-611/612 A/D boards can operate in a *fast throughput mode* for applications requiring fast data transfers. This mode is selectable using the command register. The *fast throughput mode* guarantees transfer of A/D data on to the VMEbus without having to test the conversion status. When A/D data is read, this mode delays the host CPU DTACK* while EOC = 0.

The DVME-611/612 A/D boards come with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the A/D boards. The user's manual also contains information on troubleshooting the boards

The boards are shipped with a 5.25 inch MS-DOS disk containing an example source program. Consult the factory regarding the availability of the diagnostic program's source code in other disk formats.

VME Interface

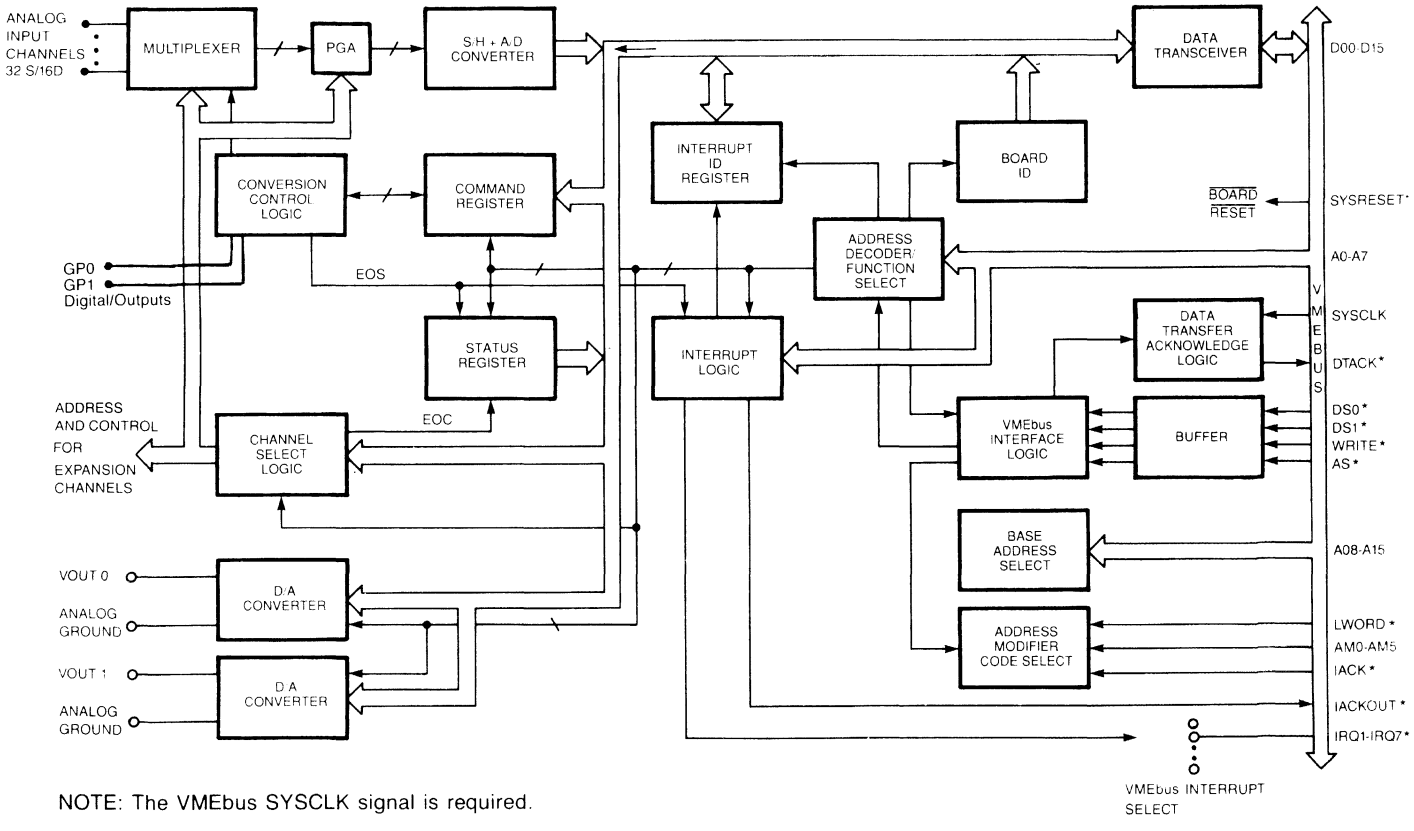
The DVME-611/612 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes.

The DVME-611/612 generates the data acknowledge (DTACK*) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK* signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes VMEbus control lines (WRITE*, DS0*, DS1*, and AS*) to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-611/612 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

VMEbus Interrupt Logic

The interrupt logic section senses an EOC or EOS condition and generates an interrupt request on one of the VMEbus interrupt lines (IRQ1* through IRQ7*). The interrupt lines are jumper-selectable. The interrupt logic accepts IACK* and IACKIN* signals from the host system as interrupt acknowledge and daisy chain input signals. Depending upon the interrupt level, the on-board logic loads the interrupt ID number on to the VMEbus or generates the daisy chain IACKOUT* signal.



NOTE: The VMEbus SYSCLK signal is required.

Figure 1. DVME-611/612 Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25 °C, unless otherwise noted)

VMEbus INTERFACE

Data Bus ..... 16 Bits. (A16:D16 slave)
Address Bus..... Short I/O Space 16 address lines
Address Modifier Codes.. Codes used 29H, 2DH, 39H, and 3DH
Interrupts ..... 1 line, jumper-selectable
2 interrupt ID's for EOC and EOS
Software programmable
Memory Mapping ..... Short I/O space, user or supervisor 256 words allocated per board
Data Transfer..... DTACK✱ signal line
Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines

ANALOG INPUT

Number of Channels..... 32 single-ended or 16 differential
Channel Expansion..... 256 single-ended or differential; requires external multiplexing. Use DATEL's DVME-641, DVME-643, or DVME-645 mux boards.
Input Configuration..... Single-ended or differential
Input Ranges ..... ±10V, ±5V, 0 to +5V, or 0 to +10V, jumper-selectable. See Table 2.
Digital Outputs
Standard..... Offset binary
Jumperable ..... Straight binary or 2's complement
External Start Trigger ..... TTL compatible, negative going edge.
Minimum pulse width = 100 nS
Maximum pulse width = 2 µS
Common Mode Voltage... ±10V dc, maximum, non-isolated
Input Bias Current..... 8 nA, maximum
Over Voltage Protection.. ±35V dc, maximum
Input Impedance
Differential to ground ..... 10 megohms, minimum

PERFORMANCE

Programmable Gain..... Uses an AM-543MC for gains of X1, X2, X4, X8, X16, X32, X64, X128
Common Mode Rejection for ±10V input signal at 60 Hz, minimum ..... 75 dB at a gain of 2
80 dB at a gain of 128
Full-Scale Range Accuracy, minimum
DVME-611A/612A..... 0.025% at a gain of 1
DVME-611E/612E..... 0.20% at a gain of 128
DVME-611B/612B..... 0.05% at a gain of 1
0.20% at a gain of 128
DVME-611C/612C..... 0.010% at a gain of 1
0.20% at a gain of 128
DVME-611D/612D..... 0.0063% at a gain of 1
0.20% at a gain of 128
DVME-611F/612F ..... 0.01% at a gain of 1
PGA plus MUX Settling Time, maximum..... 8 µS at a gain of 1
12 µS at a gain of 16
40 µS at a gain of 64
100 µS at a gain of 128

Min. conversion time
DVME-611A/612A..... 20 µS at a gain of 1
110 µS at a gain of 128
DVME-611B,E/612B,E... 8 µS at a gain of 1
102 µS at a gain of 128
DVME-611C/612C..... 35 µS at a gain of 1
110 µS at a gain of 128
DVME-611D/612D..... 400 mS at a gain of 1
400 mS at a gain of 128
DVME-611F/612F ..... 4 µS at gain = 1

Note: Allow 20 minutes warm-up for DVME-611F/612F

Resolution and Throughput

(Scan Mode)	Resolution in bits	Conversion time	Throughput conversions /sec.
DVME-611A/612A	12	20 µS	40,320
DVME-611B/612B	12	4 µS	160,000
DVME-611C/612C	16	35 µS	18,667
DVME-611D/612D	16	400 mS	2.5
DVME-611E/612E	12	2 µS	see notes
DVME-611F/612F	14	4 µS	100,000

Temperature Drift and Linearity

Model	Gain Temperature Coefficient (ppm/ °C)	Zero Temperature Drift, (ppm/ °C)	Linearity Error
DVME-611A/612A	±20	20	1/2 LSB
DVME-611B/612B	±20	20	1/2 LSB
DVME-611C/612C	±20	20	2 LSB
DVME-611D/612D	±10	10	2 LSB
DVME-611E/612E	±20	±20	1/2 LSB
DVME-611F/612F	±15	±15	2 LSB

Optional Multiplexer Expansion Boards

Model	Number of expansion channels Single-ended	Differential	Input type
DVME-641	32	16	High-level, non-isolated
DVME-643T	–	8	Thermocouple Isolated
DVME-643H	–	8	High-level Isolated
DVME-645	16	8	Simultaneous Sample/Hold high-level non-isolated

ANALOG OUTPUT (For DVME-612 models only)

Number of Channels 2
Output Range ..... ±10V, ±5V, 0 to +5V, or 0 to +10V
Digital Input Coding ..... Bipolar 2's complement, bipolar offset binary or unipolar straight binary
Resolution ..... 12 Bits, bits D0 through D3 not used
Reset ..... Minus, full-scale, -10V for 2's complement and offset binary
0V for Unipolar
Full-Scale Range
Accuracy ..... .05%, minimum
Diff. Non-Linearity ..... 0.5 LSB, minimum
Zero Temperature Drift ..... 5 ppm/ °C, maximum
Offset Temperature Drift .. 20 ppm/ °C, maximum
Gain Temperature Drift .... 20 ppm/ °C, maximum
Settling Time ..... 10 µS, maximum
Output Current ..... 5 milliamps, maximum
Output Impedance ..... 50 milliohms, typical

POWER SUPPLY REQUIREMENTS

+5V dc ±5% at 2.5 Amperes
Note: On-board dc-to-dc converter generates ±15V dc for the DVME-611/612 logic circuits

CONNECTORS

VMEbus P1 connector ..... 96-pin male DIN connector
J1 and J2 Analog Input Connectors ..... 25-pin D-type female connectors
J3 Analog Output Connector ..... 9-pin D-type female connector
J4 Analog Expansion Connector ..... 25-pin D-type female connector

PHYSICAL-ENVIRONMENTAL

Outline Dimensions ..... 9.19"W x 6.3"D x 0.6"H (233.5 x 160 x 15.24 mm)
Weight ..... 1 lb. 0.5 oz. (467.8 grams)
Operating Temp. Range ... 0 to +60 °C
Storage Temp. Range ..... -20 to +80 °C
Relative Humidity ..... 0 to 90%, non-condensing

DVME-611/612 Programming Information

The DVME-611/612 A/D boards use ten registers for data acquisition and control purposes. Table 1 lists the DVME-611/612 registers and their base address offsets. These registers are addressable locations in the host system's address space.

Address	Function	Contents
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification
Base + 128	Write	Command register (80h)
Base + 128	Read	Status register (80h)
Base + 130	Write	Interrupt ID register (82h)
Base + 132	Write	EOC/EOS F/F Reset (84h)
Base + 134	Write	Gain register (86h)
Base + 136	Write	Start channel register (88h)
Base + 136	Read	Current channel register
Base + 138	Write	Final channel register (8Ah)
Base + 140	Write	Start conversion register (8Ch)
Base + 140	Read	A/D data register
Base + 142	Read	Status register (8Eh)
Base + 160	Write	D/A channel 0 (A0h)
Base + 162	Write	D/A channel 1 (A2h)

Table 1. DVME-611/612 Hardware Register Functions

Command Register

The DVME-611/612 boards scan their selected channels under control of the 16-bit command register. Programming the command register selects the modes for starting conversion, calibration, and fast throughput. This register also enables the interrupt, channel address auto-increment, and channel re-scan capabilities. Figure 2 shows the command register format.

Status Register

The DVME-611/612 status register indicates conditions relating to conversion status, channel scanning information, and modes selected. Figure 3 shows the status register format.

Total System Throughput

Total sample-to-sample throughput rate depends on the A/D-S/H settling and conversion period and the user's software period. During the software interval, data is transferred to the host and the next A/D conversion is started. By combining fast throughput mode (DTACK* EOC holdoff) with convert-on-read-data, throughput over 400 KHz may be achieved for gain = 1 in single channel mode for model DVME-611E. Data transfer and host memory pointer management may partially overlap A/D Conversion by using the convert-on-read mode.

Fast Throughput Mode

This mode holds off response of the DTACK* VMEbus signal with the simultaneous ANDing of three conditions: command register bit 5 = 1, EOC = 0, and a host read of the A/D data register. While DTACK* is held off, the host CPU executes wait states. When A/D conversion finishes, EOC = 1 and DTACK* is released. Normally the attempted A/D data read now completes, and data is transferred without any EOC polling. Fast throughput should be used with caution since the host must be completely dedicated to A/D data acquisition.

Table 2. A/D Full Scale Input Ranges (PGA gain = 1)

Input Range	Model 611/612A	611/612B,E	611/612C	611/612D	611/612F
0 to +5V	X	NA	NA	NA	NA
0 to +10V	X	X	NA	NA	S
±5V	X	NA	X	NA	S
±10V	X	X	X	X	X

X = supplied. NA = not available. S = solderable on module

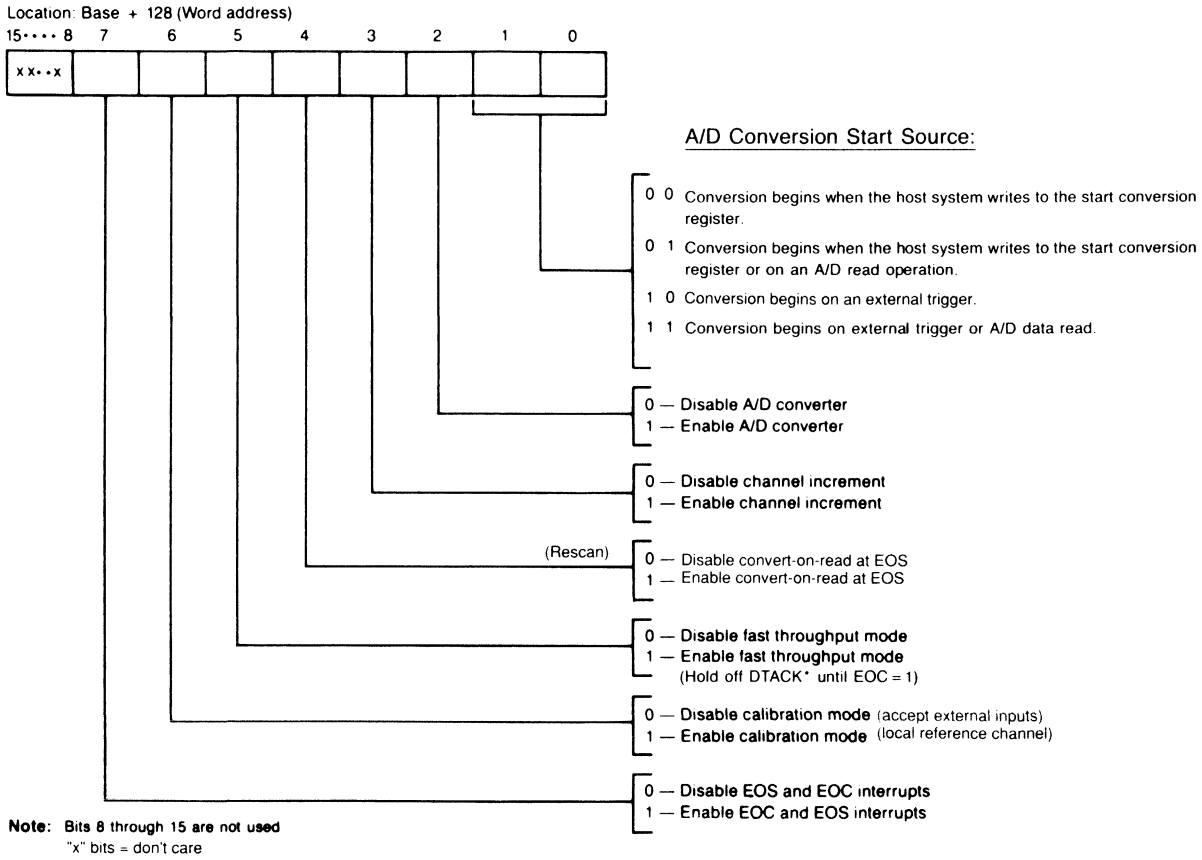


Figure 2: DVME-611/612 Command Register Format (WRITE)

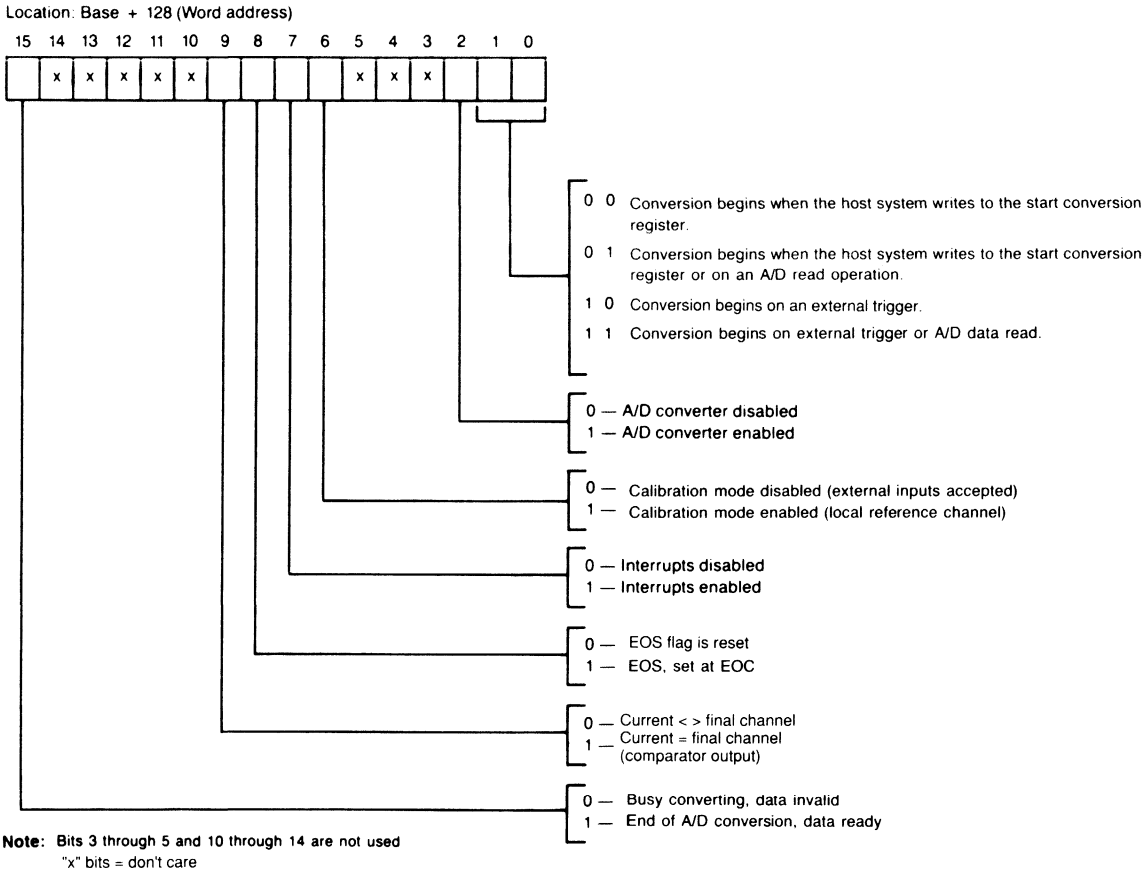


Figure 3: DVME-611/612 Status Register Format (READ)

Interrupt ID Register

This register contains the user-loaded interrupt ID number. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK★ and the daisy chain IACKIN★ signal lines. If the DVME-611/612 interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number on to the VMEbus (low byte). If the EOC/EOS interrupts and the multiple channel scan option are enabled, the board loads the ID number plus one on to the VMEbus data lines. The host system may use these ID's to differentiate the EOC and EOS interrupts. Figure 4 shows the register format of the interrupt ID register.

Word address: Base + 130 (Write) X = Don't Care

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	ID7	ID6	ID5	ID4	ID3	ID2	ID1	0

Figure 4: Interrupt ID Register Format

Gain Register and Digital Outputs

The least three significant bits of this register, when programmed, assign the gain to the differential amplifier in the PGA section. This register is programmable for gains from 1 to 128 in binary increments. Bits 6 and 7 of this register provide a general purpose digital output. The output signal lines from these two bits are available on pins 18 and 6 of the J4 connector. Figure 5 shows the gain register format.

Word address: Base + 134 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	GP1	GP0	x	x	x	G2	G1	G0

Figure 5: Gain Register Format

Start Channel/Current Channel Register

User must load this register with the starting channel address when scanning a group of channels. This register contains the address of the channel being scanned. Figure 6 shows the format of this register.

Word address: Base + 136 (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Figure 6: Start Channel/Current Channel Register

Final Channel Register

User must load this register with the final channel address when scanning a group of channels. The on-board comparator compares this register contents with the current channel register and generates the end of scan (EOS) signal. Figure 7 shows the format of this register.

Word address: Base + 138 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Figure 7: Final Channel Register Format

Start Conversion Register

Writing any value to this register starts an A/D conversions on the channel indicated by the current channel register. Figure 8 shows the format of this register.

Word address: Base + 140 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Figure 8: Start Conversion Register Format

A/D Data Register

The 16 bits of the A/D data register are connected to 16 VMEbus data lines. The host system may read this register to obtain the binary data of the analog input from the channel selected. Models DVME-611/612 A, E, and B do not use the four least significant data bits. The value of these bits defaults to zero for these models. Figure 9 shows the format of this register.

Word address: Base + 140 (Read)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13	AD14	AD15	AD16

MSB (Data is left-justified) LSB

Figure 9: A/D Register Format

D/A Channel Registers

The DVME-612 boards have two D/A channel registers. These registers form the input to the 12-bit hybrid D/A converters. These registers are programmable by the most significant 12 bits from the VMEbus data lines. Figure 10 shows the format of these registers.

Word address: Base + 160 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x

MSB LSB

Figure 10a: D/A Channel 0 Register Format

Word address: Base + 162 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x

MSB LSB

Figure 10b: D/A Channel 1 Register Format

EOC/EOS F/F Register

Writing any value to this register resets the EOC/EOS flip-flops. Figure 11 shows the format of this register.

Word address: Base + 132 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Figure 11: EOC/EOS F/F Register Format

(These F/F's are also reset by the next start of conversion or by reading A/D data.)

I/O Connections

The DVME-611/612 A/D boards use the J1 and J2 connectors for analog input connections and the J4 connector for channel expansion. The DVME-612 uses the J3 connector for analog output connections. Tables 2, 3, 4, and 5 list the I/O signals of the J1, J2, J3, and J4 connector respectively.

Table 3. DVME-611/612 Analog Input Connector - J1

	CONFIGURATION	
PIN #	SINGLE-ENDED	DIFFERENTIAL
24	CHANNEL 0 IN	CHANNEL 0 HIGH
12	CHANNEL 16 IN	CHANNEL 0 LOW
25	ANALOG RETURN	ANALOG RETURN
10	CHANNEL 1 IN	CHANNEL 1 HIGH
23	CHANNEL 17 IN	CHANNEL 1 LOW
11	ANALOG RETURN	ANALOG RETURN
21	CHANNEL 2 IN	CHANNEL 2 HIGH
9	CHANNEL 18 IN	CHANNEL 2 LOW
22	ANALOG RETURN	ANALOG RETURN
7	CHANNEL 3 IN	CHANNEL 3 HIGH
20	CHANNEL 19 IN	CHANNEL 3 LOW
8	ANALOG RETURN	ANALOG RETURN
18	CHANNEL 4 IN	CHANNEL 4 HIGH
6	CHANNEL 20 IN	CHANNEL 4 LOW
19	ANALOG RETURN	ANALOG RETURN
4	CHANNEL 5 IN	CHANNEL 5 HIGH
17	CHANNEL 21 IN	CHANNEL 5 LOW
5	ANALOG RETURN	ANALOG RETURN
15	CHANNEL 6 IN	CHANNEL 6 HIGH
3	CHANNEL 22 IN	CHANNEL 6 LOW
16	ANALOG RETURN	ANALOG RETURN
1	CHANNEL 7 IN	CHANNEL 7 HIGH
14	CHANNEL 23 IN	CHANNEL 7 LOW
2	ANALOG RETURN	ANALOG RETURN

Table 4. DVME-612 Analog Output Connector - J3

PIN #	SIGNAL LINE
1	CHANNEL 0 VOUT
6	ANALOG RETURN
4	CHANNEL 1 VOUT
9	ANALOG RETURN

Table 5. DVME-611/612 Analog Input Connector - J2

	CONFIGURATION	
PIN #	SINGLE-ENDED	DIFFERENTIAL
24	CHANNEL 8	CHANNEL 8 HIGH
12	CHANNEL 24	CHANNEL 8 LOW
25	ANALOG RETURN	ANALOG RETURN
10	CHANNEL 9	CHANNEL 9 HIGH
23	CHANNEL 25	CHANNEL 9 LOW
11	ANALOG RETURN	ANALOG RETURN
21	CHANNEL 10	CHANNEL 10 HIGH
9	CHANNEL 26	CHANNEL 10 LOW
22	ANALOG RETURN	ANALOG RETURN
7	CHANNEL 11	CHANNEL 11 HIGH
20	CHANNEL 27	CHANNEL 11 LOW
8	ANALOG RETURN	ANALOG RETURN
18	CHANNEL 12	CHANNEL 12 HIGH
6	CHANNEL 28	CHANNEL 12 LOW
19	ANALOG RETURN	ANALOG RETURN
4	CHANNEL 13	CHANNEL 13 HIGH
17	CHANNEL 29	CHANNEL 13 LOW
5	ANALOG RETURN	ANALOG RETURN
15	CHANNEL 14	CHANNEL 14 HIGH
3	CHANNEL 30	CHANNEL 14 LOW
16	ANALOG RETURN	ANALOG RETURN
1	CHANNEL 15	CHANNEL 15 HIGH
14	CHANNEL 31	CHANNEL 15 LOW
2	ANALOG RETURN	ANALOG RETURN

Table 6. DVME-611/612 Expansion Connector - J4

PIN #	SIGNAL LINE
13	EXTERNAL CHANNEL ADDRESS 0 OUT
25	EXTERNAL CHANNEL ADDRESS 1 OUT
12	EXTERNAL CHANNEL ADDRESS 2 OUT
24	EXTERNAL CHANNEL ADDRESS 3 OUT
11	EXTERNAL CHANNEL ADDRESS 4 OUT
23	EXTERNAL CHANNEL ADDRESS 5 OUT
10	EXTERNAL CHANNEL ADDRESS 6 OUT
22	EXTERNAL CHANNEL ADDRESS 7 OUT
16	DIGITAL GROUND
9	EXTERNAL CHANNEL ADDRESS VALID OUT
8	START CONVERSION STROBE OUT
20	SETTLING DELAY★ IN
7	END OF CONVERSION OUT
19	END OF SCAN OUT
17	EXTERNAL TRIGGER IN*
18	GENERAL PURPOSE OUTPUT 0
6	GENERAL PURPOSE OUTPUT 1
4	DIGITAL GROUND
21	RESERVED
5	RESERVED
1	EXTERNAL ANALOG LOW IN
14	EXTERNAL ANALOG HIGH IN
2, 15	ANALOG COMMON
3	+5V dc REFERENCE OUT (5mA)

DVME-611/612 Board Indentification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+3	M	This ASCII code is present
+5	E	for all DATEL VMEbus boards
+7	I	
+9	D	
+0B	D	Manufacturer ID
+0D	A	DAT is the ID for DATEL
+0F	T	
+11	d	Board model number
+13	V	
+15	M	
+17	E	
+19	–	
+1B	6	
+1D	1	
+1F	1 or 2	

ORDERING INFORMATION

DVME-611 (A/D only)
DVME-612 (A/D + D/A)

- A - 12-bit/20 µS ADC
- B - 12-bit/4 µS ADC
- C - 16-bit/35 µS ADC
- D - 16-bit/400 mS
- E - 12-bit/2 µS ADC
- F - 14-bit/4 µS

Optional Multiplexer Expansion Boards

DVME-641 - 32S/16D Channel high-level non-isolated inputs.
DVME-643 - 8D Channel isolated inputs.
DVME-645 - 16S/8D Channel simultaneous sample/hold high-level non-isolated inputs.

Accessories

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer)
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards)

Each board includes a disk and manual.

DATEL VMEbus Short I/O Memory Organization

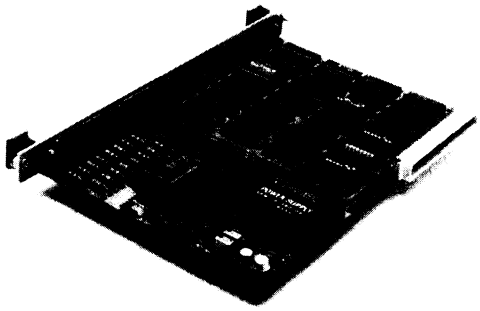
Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base +64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	Not used	
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended; 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples, RTD's, strain gages, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	Not used	
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board
Base + 176 through Base + 191	Not used	
Base + 192 through Base + 255	Not used	

For an intelligent A/D board (local 68010, dual port RAM, RS-232, etc.), see model DVME-601.

DVME-613
Isolated Industrial 16S or 8D-Channel VME A/D Board

FEATURES

- **16 Single-ended or 8 differential analog input channels**
- **12-, 14- or 16-Bit A/D resolution**
- **Isolation to ±500V**
- **On-board programmable gain amplifier and start timer**
- **8 In and 8 out discrete digital lines**
- **Programmable vectored VME interrupt**
- **Simple programming for any operating system or language**



GENERAL DESCRIPTION

Designed for industrial data acquisition, process control, and factory automation, the DVME-613 is an isolated analog input board for VMEbus computers. The DVME-613 will accept sixteen single-ended or eight differential input channels which are all isolated from the VMEbus by ±500 Volts. In addition, each channel is protected from adjacent channel overloads up to ±150 Volts. The common mode voltage range is ±11 Volts relative to isolated analog ground.

The analog input range is selectable as ± 10 Volts for bipolar inputs or 0 to +10 Volts unipolar. By using an on-board programmable gain amplifier (PGA), inputs may be accepted directly from bridges, load cells, RTD's, and strain gauges. The PGA includes selectable gain ranges of times one, ten and one hundred for low level inputs.

An optional signal conditioning pad area accepts shunt resistors, attenuators, hash filters, and clamps. This allows direct input from isolated 1-5 mA or 4-20 mA transmitters and from voltage sources greater than ± 10 Volts full scale. For bridge-type sensors, on-board regulated DC excitation voltage is provided which is fully isolated from VMEbus.

The DVME-613 inputs are plug compatible with DATEL's DVME-691 rack-mount signal conditioning panel for screw terminal inputs. Three A/D converter options are offered. The DVME-613A is a 12-bit A/D converter with overall accuracy of ±0.05% of full scale. Resolution of the DVME-613A is 2.5 millivolts per count for unipolar inputs.

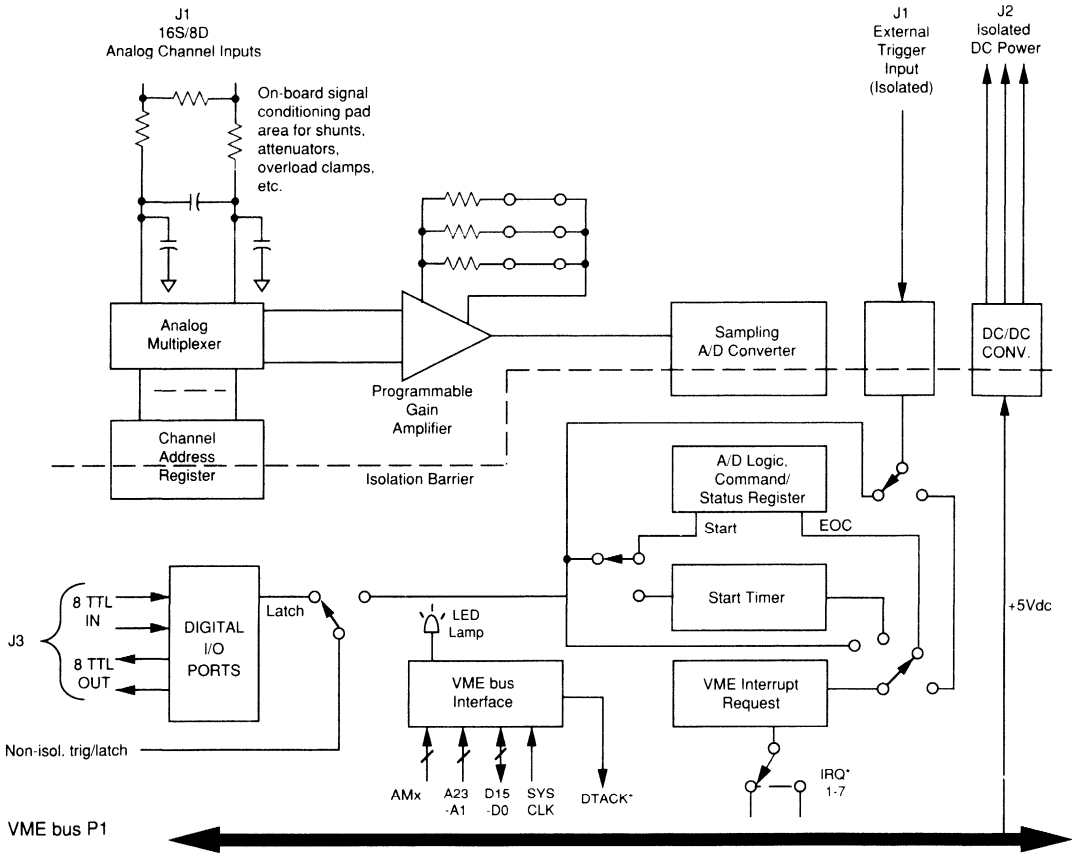


Figure 1. DVME-613 Simplified Block Diagram

GENERAL DESCRIPTION (Cont.)

The DVME-613B offers a 14-bit A/D converter and for highest resolution inputs, a 16-bit converter is included on the DVME-613C. All models produce left-justified data outputs. A/D conversion takes 24 microseconds for the DVME-613A. The sampling A/D converter design offers continuous automatic recalibration. To insure reliability in industrial process control enviroments, local channels may be dedicated to ground and reference inputs for self-testing of signal paths.

A/D conversion may be started from several sources including an external isolated trigger input, the local start timer, a memory write from the host or a read of the A/D data register. The maskable vectored VMEbus interrupt may originate from an external trigger, the local timer or the A/D EOC data ready signal.

VMEbus interrupts are fully vectored using selectable IRQ 1-7 levels.

The A/D data ready EOC signal is indicated in a status register and maskable VMEbus interrupt. All modes are software controlled by local command and status registers.

The DVME-613 provides 16 digital lines for logic control of devices such as pumps, heaters and valves. These lines are TTL logic compatible and arranged as eight inputs and eight outputs. A separate control input latches the eight TTL input lines.

The DVME-613 is a VMEbus SA24:SD16 slave. The board appears to the VMEbus as a memory-mapped 8-word contiguous block of 16-bit registers using 24-bit addressing and six address modifiers. All types of 16- and 32-bit host CPU's may control the board on 16-bit word access using any software language.

The VMEbus interface uses only the P1 backplane connector for compatibility with most hosts. All analog and digital port interfacing uses front panel connectors to avoid conflict with P2 bus connector usage. A front panel LED lamp may be programmed by host software for board power-up test or for alarms.

Operating temperature range of the DVME-613 is 0 to +60 °C. The board measures 9.19" x 6.3" x 0.6", using the standard 6U VMEbus outline. All power is supplied by VMEbus requiring +5 Volts DC at 2.5 Amps.

The board includes a free software program disk and a comprehensive user's manual. The source-code software is heavily commented and may be easily adapted for any operating system or host language. Application engineering consultation is available to users.

FUNCTIONAL SPECIFICATIONS

(Specifications are for the total system and are typical at +25 °C, gain=1 unless noted)

ANALOG INPUTS

Number of Channels		8 differential or 16 single-ended	
Full Scale Input Ranges		**Unipolar**	**Bipolar**
	Gain = 1	0 to 10V	±10 V
	Gain = 10	0 to 1V	±1 V
	Gain = 100	0 to 100mV	±100 mV
Input Isolation		±500V max. from analog section to VMEbus	
Isolation Capacitive Coupling		25 pF analog section to VME	
Isolation Resistive Coupling		100 MΩ analog to VME	
Common Mode Voltage Range		± 11V to isolated ground	
Common Mode Rejection		86 dB, dc to 60 Hz, gain=100, 1KΩ source unbalance	
Channel-to-Channel Protection		±150V max. sustained	
Input Bias Current		±200 picoamps	
Input Impedance (power on)		100 MΩ to isolated ground	
Input Impedance (power off)		33 KΩ to isolated ground	
Programmable Gain Amplifier		Jumper selectable for gains of 1, 10 or 100. Will accept precision resistor for user defined gain	
PGA Settling Delay		10 µS, gain=1 (after channel selection); 20 µS, gain=10; 100 µS, gain=100	
A/D Output Resolution		12 binary bits (DVME-613A) 14 binary bits (DVME-613B) 16 binary bits (DVME-613C)	
A/D Output Coding		Selectable as unipolar straight binary or bipolar offset binary	
Accuracy at +25 °C (After recalibration)	(Gain = 1 or 10)	DVME-613A:	±0.05% of FSR
	(Gain = 100)	DVME-613A:	±0.1% of FSR
	(Gain = 1)	DVME-613B:	±0.0125% of FSR
	(Gain = 1)	DVME-613C:	±0.0075% of FSR
Nonlinearity		± 0.5 LSB	
Temperature Coefficient of Zero		±20 ppm/ °C of FSR	
Temperature Coefficient of Gain		±20 ppm/ °C of FSR	
A/D Conversion Period		613A: 24 µS* 613B: 28 µS* 613C: 32 µS*	
A/D Converter Start Sources		External isolated TTL trigger, local pacer start clock, VME command write, or VME A/D data read. The TTL trigger occurs on the rising edge. Trigger width 0.1 to 5 µS	
Monotonicity		No missing codes	

DIGITAL SECTION

A/D Start Clock	May be jumpered to start an A/D conversion /VMEbus interrupt
Start Clock Range	32 µS to 5 minutes, jumperable in x2 steps. Derived from 16 MHz VMEbus SYSCLK.
Discrete I/O Lines	8 inputs and 8 outputs, non-isolated, latch control for inputs
Discrete I/O TTL Levels	Inputs: "0" < 0.8V, "1" > 2.0V Outputs: "0" < 0.4V, "1" > 2.4V
Discrete TTL I/O Loading	1 TTL-LS load plus 4.7 KΩ pullup to +5V outtput: Output: 24 mA
LED Lamp	Front panel lamp software controlled by register bit. May be used for power up test, alarms, etc. Defaults to dark at power up or bus reset.

VMEbus INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Architecture	SAD24:SD16 slave consisting of 8 contiguous word registers.
Data Bus Width	16 bits using P1 connector.
Address Bus	24 address lines (A23-A1) plus 6 Address Modifiers.
Address Modifier Codes	39 or 3D hex, selectable
VMEbus Interrupt	1 line, selectable IRQ 1-7*. Asserts maskable programmable 8-bit vector ID code.
Interrupt Source	Selectable from external trigger, start timer or A/D data ready.
Data Transfer	Uses 16 MHz VMEbus SYSCLK signal to generate DTACK* signal with selectable delay.

CONNECTORS	
VMEbus, P1	96-pin male DIN connector. The P2 connector is not used.
Local Isolated Analog Input and Isolated Trigger	J1 connector, 25-pin DB-25S female on front panel, pin-compatible to DVME-691 screw terminator.
Isolated DC Power	J2 connector, 25-pin DB-25S female on front panel. Power available: ±15V dc at 25 mA max.
Discrete Digital I/O	J3 connector, 25-pin DB-25S female on front panel.

MISCELLANEOUS	
Power Required	+5V dc ±5% at 2.5 Amps max. from VMEbus.
Operating Temperature Range	0 to +60 °C
Storage Temperature Range	-20 to +80 °C
Relative Humidity	10 to 90%, non-condensing
Altitude	0 to 10,000 feet.
Outline Dimensions	Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233,5 x 160 x 15,24 mm)
Weight	17 ounces (482 grams)

*Single channel conversion rates are shown. For multichannel inputs, an additional 20 µS must be allowed after channel selection before the next A/D conversion start.

TYPICAL BRIDGE-TYPE INPUT CONNECTIONS

Figure 2 shows the DVME-613 connected to a bridge-type transducer. Notice that the bridge excitation is derived from the +15V dc power available from the DVME-613. The excitation voltage is regulated but not extremely high-precision.

To compensate for this, use a precision voltage divider and measure the excitation supply using a spare differential channel. Then use this value to do a software autocalibration with each channel scan.

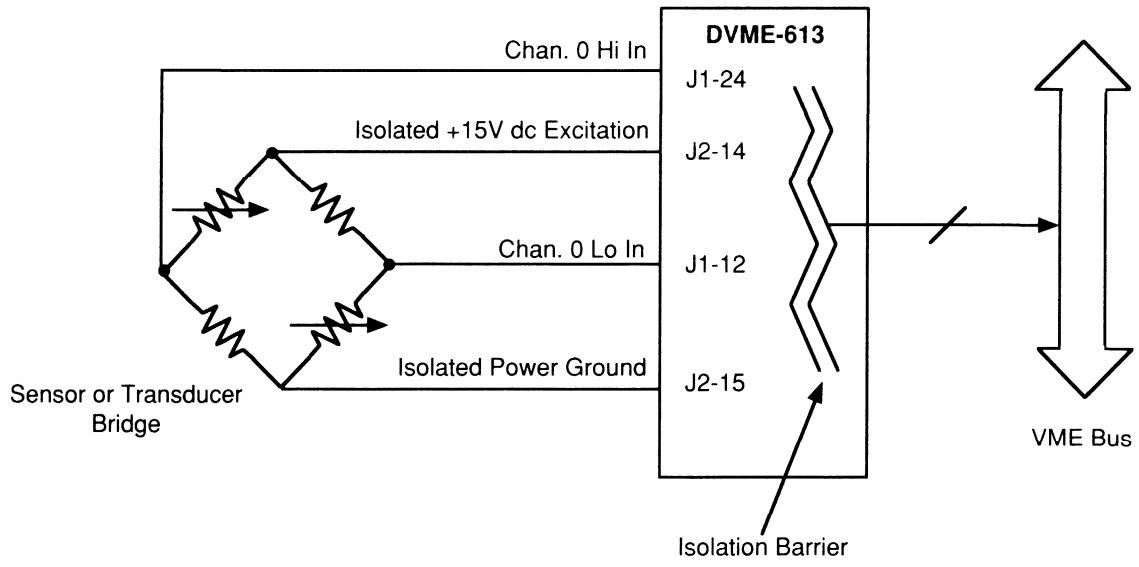


Figure 2. Typical Bridge-type Input Connections

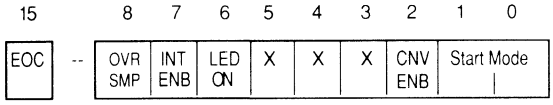
REGISTER PROGRAMMING

Register Memory Mapping

BASE address switches must be selected for even address boundaries. All registers must be accessed on 16-bit word memory operations.

Address (Hex)	Direction	Description
BASE+0	Write	Command register
BASE+0	Read	Status register
BASE+2	Write	Channel address register
BASE+4	Write	Start A/D conversion register
BASE+6	Read	A/D data register
BASE+8	Write	Interrupt vector ID register
BASE+8	Read	Interrupt vector ID register
BASE+A	Write	Calibrate A/D converter
BASE+C	Write	TTL digital output port register
BASE+E	Read	TTL digital input port register

Command/Status Register (Write/Read BASE+0)



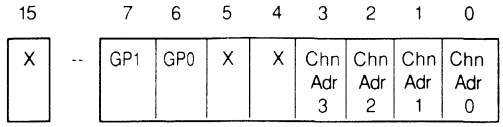
("x" bits are don't care or not defined)

If interrupt is not used, the host should poll EOC before reading A/D data. The read of the A/D data register resets EOC to 0 even if another conversion is not started.

EOC (bit 15) read only End of A/D Conversion	0 = Conversion in progress. Data not valid 1 = Conversion done. Data ready
OVR SMP (bit 8) read only Over Sample Error	0 = No error 1 = Oversampling error (conversion start while EOC=0, A/D busy)
INT ENB (bit 7) R/W VME Interrupt Enabled	0 = Interrupt disabled 1 = Interrupt enabled (Interrupts may be jumpered from A/D EOC, external trigger or internal timer)
LED (bit 6) R/W Front panel lamp	0 = LED lamp off 1 = LED lamp on
CNV ENB (bit 2) R/W A/D Conversion Enabled	0 = Disable A/D conversions 1 = Enable A/D conversions
A/D Start Mode (bits 1,0) R/W	Source of A/D start: 00 = Host write to BASE+4 01 = Read A/D data register 10 = Internal start timer 11 = External TTL trigger

Program the command register last. All registers default to zeroes at power-up.

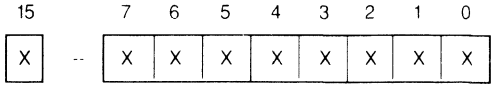
Channel Address Register (Write BASE+2)



GP1, GP0 (bits 7,6) - These are spare unassigned register output bits available for any purpose. They appear at integrated circuit U19-10,12.

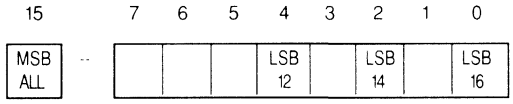
Chn Adr (bits 3-0) - Channel Address input corresponding to A/D channels 0 through 7 (differential) or 0 through 15 (single-ended).

Start A/D Conversion Register (Write BASE+4)



An A/D conversion may be started by a write to this register if enabled by the command register mode 00. EOC will be set to 0 after conversion is started and until data is ready.

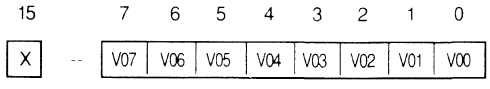
A/D Data Register (Read BASE+6)



A/D data is left justified for all converters. The least significant bit for the 12-bit DVME-613A is bit 4 with bits 3-0 filled with zeroes. The LSB for the 14-bit DVME-613B is bit 2 with zero fill. For the 16-bit DVME-613C, the LSB is bit 0.

For bipolar converters, the MSB is used as a polarity bit and is set to offset binary (1 = positive).

VMEbus Interrupt Vector ID Register (Read/Write BASE+8)



An 8-bit interrupt ID code is used. Before writing the ID code from the host, this register may be used for board testing. A valid power-up test would be to write then readback and confirm a range of values to this register before enabling interrupts. Portions of the command/status register may also be used for write/readback tests. Such tests would confirm the bus interface and register logic. Further testing may be done using the dedicated reference inputs to the A/D converter. If all tests succeed, the front panel LED lamp may be lit.

Calibrate A/D Converter (Write BASE+A)

15	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X

Writing to this register will start an A/D calibration cycle for approximately 320 milliseconds until EOC. This operation should be done once after power up. During calibration, the A/D converter makes internal corrections. Periodic calibration is optional in stable temperature environments but is suggested frequently with changing temperatures.

Discrete Digital Output Register (Write BASE+C)

15	7	6	5	4	3	2	1	0
X	D07	D06	D05	D04	D03	D02	D01	D00

Discrete Digital Input Register (Read BASE+E)

15	7	6	5	4	3	2	1	0
X	D07	D06	D05	D04	D03	D02	D01	D00

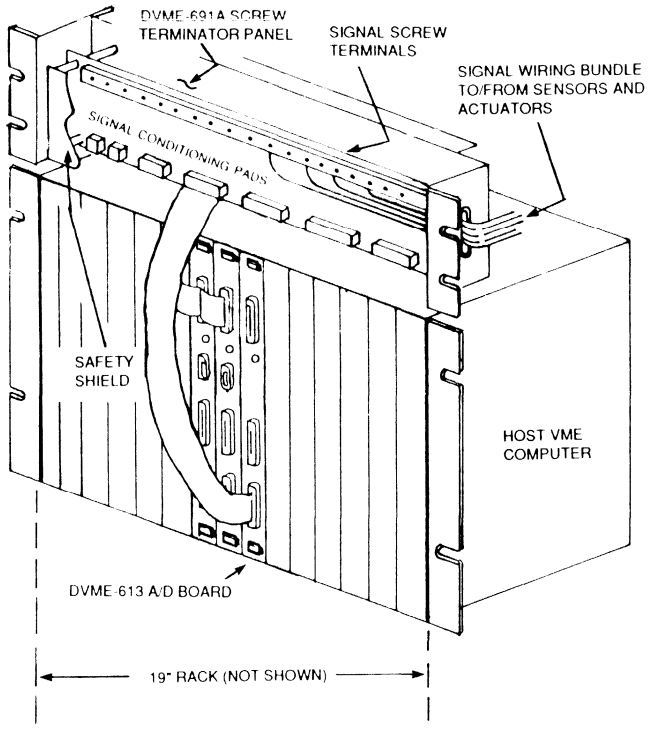


Figure 3. Cabling the DVME-613 Using DATEL's DVME-691 Screw Terminator Panel

FRONT PANEL INPUT/OUTPUT CONNECTIONS

Pin numbering is shown as viewed from the front panel.

Discrete Non-isolated Digital I/O - Connector J3

Digital Out 7	25	13	13	External Trig*/ Latch In
Digital Out 6	24	12	12	Digital Ground
Digital Ground	23	11	11	Digital Out 5
Digital Out 3	22	10	10	Digital Out 4
Digital Out 2	21	9	9	Digital Ground
Digital Ground	20	8	8	Digital Out 1
Digital In 7	19	7	7	Digital Out 0
Digital In 6	18	6	6	Digital Ground
Digital Ground	17	5	5	Digital In 5
Digital In 3	16	4	4	Digital In 4
Digital In 2	15	3	3	Digital Ground
Digital Ground	14	2	2	Digital In 1
		1	1	Digital In 0

Isolated DC Power Out - Connector J2

Non-Isol. Dig. Ground	25	13	13	Non-Isol. Digital Ground
+5V dc Out (non-isol.)	24	12	12	+5V dc Out (non-isol.)
No Connection	23	11	11	No Connection
No Connection	22	10	10	No Connection
No Connection	21	9	9	No Connection
No Connection	20	8	8	Spare to internal pad
No Connection	19	7	7	Spare to internal pad
No Connection	18	6	6	Spare to internal pad
No Connection	17	5	5	Spare to internal pad
-15V dc Out (<25 mA)	16	4	4	No Connection
Isolated Ground	15	3	3	-15V dc Out (<25 mA)
+15V dc Out (<25 mA)	14	2	2	Isolated Ground
		1	1	+15V dc Out (<25 mA)

Isolated Analog Inputs - Connector J1

Signal Ground	25	13	13	Isol. External Trigger In
Chan. 0 Hi	24	12	12	Chan. 8 Hi/Chan. 0 Lo
Chan. 9 Hi/Chan. 1 Lo	23	11	11	Signal Ground
Signal Ground	22	10	10	Chan. 1 Hi
Chan. 2 Hi	21	9	9	Chan. 10 Hi/Chan. 2 Lo
Chan. 11 Hi/Chan. 3 Lo	20	8	8	Signal Ground
Signal Ground	19	7	7	Chan. 3 Hi
Chan. 4 Hi	18	6	6	Chan. 12 Hi/Chan. 4 Lo
Chan. 13 Hi/Chan. 5 Lo	17	5	5	Signal Ground
Signal Ground	16	4	4	Chan. 5 Hi
Chan. 6 Hi	15	3	3	Chan. 14 Hi/Chan. 6 Lo
Chan. 15 Hi/Chan 7 Lo	14	2	2	Signal Ground
		1	1	Chan. 7 Hi

Channel address notation: Single-ended/Differential

PROGRAMMING

The DVME-613 appears to the host computer as a block of 16-bit memory-mapped registers. To program the DVME-613, read/write memory word operations may be used from any language. In "C", short pointers will access these registers. In 680X0 assembly language, move word (move.w) operations do the job. Since the DVME-613 is addressed as absolute memory, any host language or operating system may be used. In UNIX, a library function may be needed to map absolute physical addresses to logical addresses.

Either polled status bits or interrupts may be used to indicate when A/D data is ready. If you wish to use interrupts, a simple device driver may be used to send a flag to the Operating System. A device driver is not necessary for polled operation.

A sample "C" program to control the DVME-613 is listed below:

```
/* 613c.c demo 4may89 ldc */

#include <stdio.h>
#include <io.h>

#define SAMPLES 8 /* last channel + 1 to scan */

/* The base address below is set by board switches before
installation. Change this base address for your system: */

#define BASPTR 0xFF0000 /* 24-bit address */

/* Make sure all shorts declared below refer to 16-bit words */

unsigned short *base_ptr; /* base address */

/* offsets to board registers: */
unsigned short *ctl_ptr, /* command-status */
   *chan_ptr, /* channel address */
   *start_ptr, /* start conversion */
   *addat_ptr; /* A/D data */

unsigned short outdata[8]; /* array to store A/D samples */
int scan(int samples), channel, wait(int delay);

main(){
    /* initialize pointers to registers.
   Note pointer (cast) */
   base_ptr = (unsigned short *) BASPTR;
   ctl_ptr = (unsigned short *) (BASPTR + 0);
   chan_ptr = (unsigned short *) (BASPTR + 2);
    addat_ptr = (unsigned short *) (BASPTR + 6);

   scan(SAMPLES);
   printf("\nA/D data (hex):");
   for( channel=0 ; channel < SAMPLES ; channel++ )
      printf("\nChan. %d = %x", channel, outdata [channel] );
} /* end of main */

/*   Functions
*/

wait(delay){
while(delay--)
    ;
}
/* Scan()  collects one scan of A/D samples to outdata[ ] with
sequential channel addressing starting at channel 0. */

scan(samples){
    int channel = 0; /* current channel address started at 0 */

   /* Initialize command register, no interrupts, LED on,
   converter enabled, trigger on A/D data read: */
    *ctl_ptr = 0x0045;
    *chan_ptr = 0; /* start at channel 0 */
   wait(10); /* Adjust this for a 20-microsecond minimum set-
tling delay whenever the channel address is changed */

   /* Do one dummy A/D read to start conversion. This sample
will be overwritten: */
   outdata [channel] = *addat_ptr;

   while( channel < samples ) {
      /* wait for EOC true */
      while(( 0x8000 & *ctl_ptr ) != 0x8000 )

      *chan_ptr = channel + 1; /* bump channel address */
      wait(10); /* settling delay */
      /* store the last channel and start the next one */
      outdata [channel++] = *addat_ptr;
```

Ordering Guide

Model	Description
DVME-613A	12-bit A/D board
DVME-613B	14-bit A/D board
DVME-613C	16-bit A/D board

All models include a comprehensive user's manual and a software disk. All boards are burn-in tested under power-cycled conditions and include a one-year warranty. Datel will review custom signal conditioning for quantity requirements.

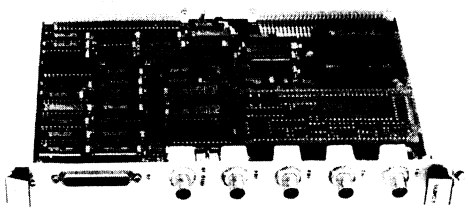
Accessories

DVME-691A Screw terminator panel for 19-inch rack mount. Includes flat signal cables to the DVME-613.

DVME-614
High Speed Analog Input Board for VMEbus Computers

FEATURES

- **Up to 4 MHz A/D sample rate**
- **Choice of 12- or 14-bit A/D resolution**
- **Optional 4 simultaneous sample/hold's**
- **On-board FIFO memory for up to 4096 samples**
- **Very low harmonic distortion**
- **Ideal for FFT's, DSP or array processor "front ends"**
- **Non-Bus burst parallel port for seamless non-stop recording.**
- **Analog input comparator trigger**



GENERAL DESCRIPTION

Offering very high system speed, the DVME-614 is a multi-channel analog input board for VMEbus computers. Single channel full power input bandwidth is available up to 2.5 MHz and may be sampled up to 4 MHz.

The single-ended analog input ranges of the A/D converter are selectable as unipolar 0 to +10 Volts, or bipolar ±5 Volts, or ±10 Volts depending on model. The gain on the DVME-614A may be user-selected times one or times ten on two channels. The DVME-614E offers 16 single-ended or 8 differential inputs and programmable gain up to times 100.

Model DVME-614A uses a Simultaneous Sample/Hold section (SSH). The SSH acquires signals on parallel channels at the same time then the A/D converter rapidly digitizes each held signal sequentially. This provides phase correction and deskewing of multichannel correlated signals.

A/D data passes to an on-board First-In, First-Out (FIFO) data memory. The design can continuously collect analog data with non-stop converter triggering while data is simultaneously read from the FIFO. Functions such as FFT sampling cannot tolerate lost samples without increases in "arithmetic" noise during computation processing. The FIFO decouples the precise timing of the A/D section to conform with the block-oriented data transfers to the bus. Data may be transferred to mass storage peripherals such as disk or magnetic tape via the host computer bus interface under host software control.

The FIFO data output may also be routed under host software control to an on-board parallel digital data port. The parallel outport uses a universal ready/acknowledge transfer handshake adaptable to any remote parallel port. Typically, a FIFO half-full interrupt from the DVME-614 triggers an external processor to burst a fixed length block of samples.

The analog section of the DVME-614 is optimized for high signal quality and very low dynamic noise. The board is de-

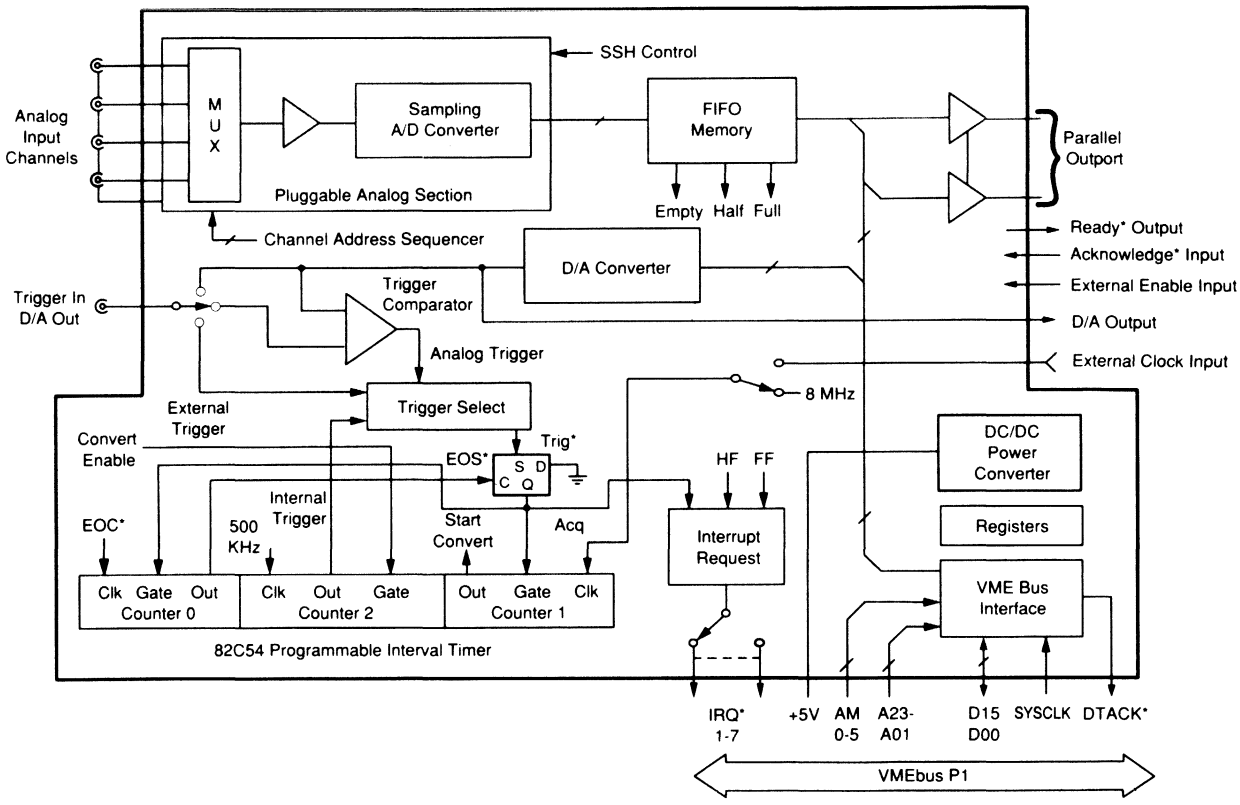


Figure 1. DVME-614 Block Diagram

signed and qualified with low Total Harmonic Distortion (THD) characteristics. The DVME-614 is ideal as an FFT "front end" or DSP quantizer.

The A/D conversion timing section is designed for accurate multi-scan data acquisition. Software programmable timers control the interval between each conversion and each multi-channel scan. A programmable sample counter allows sample blocks of specified length independent of FIFO length. The timer/counter section uses a precision on-board VMEbus clock and may be replaced by an external timebase. Timeout and sample count activities may be monitored from the computer bus using I/O status registers and/or programmable interrupts.

S/H-A/D triggering may use several sources under software control. The internal timebase is the normal trigger source although single conversions or scans may be directly commanded by host I/O register writes. An external trigger clock may also be used to precisely synchronize sampling with external events. This external trigger may start a single sample, a single multichannel scan, or "N" multiple scans separated by programmable delays.

Analog sampling may also be level-triggered using an on-board analog comparator. The reference trigger level to the comparator is derived from an on-board 12-bit D/A converter. If preferred, the D/A converter may also be used as an analog output channel for any purpose.

The DVME-614 A-D have five front panel signal connectors. Four connectors are for the sampled analog channels. The fifth connector is for a choice of the external timebase clock input, the external analog trigger level or for the D/A output. The DVME-614E uses a 25-pin connector. The computer interface for control and status uses 24-bit addressing. Board control and A/D data uses 16-bit VMEbus transfers. A single interrupt is generated for a variety of conditions under host software control. These include A/D data ready, sample count reached, FIFO half-full or FIFO full.

A/D output data coding is right-justified two's complement with sign extension. This format is excellent for integer data typing with high level computer languages such as "C", FORTRAN, Pascal or Ada. It is also directly compatible with very fast arithmetic instructions for all microprocessor assembly languages and math coprocessors. Straight binary coding may also be selected.

A high-efficiency, low noise DC/DC converter provides quiet power to linear sections. The burst channel parallel port uses a 25-pin "D" front panel connector.

The DVME-614 is supplied with a set of low level device driver examples in assembly language and "C". These are supplied on universal 5.25" MS-DOS disks. The drivers may be adapted to most host Operating Systems. The user manual has register and timing information for programmers to write their own software for any CPU or operating system. The drivers may operate in either interrupt or status mode.

DVME-614 FEATURE/BENEFIT SUMMARY

DESIGN FEATURE	BENEFIT	APPLICATIONS
Common motherboard with small, pluggable analog input modules.	Various S/H and A/D speed and resolution options available.	High-speed, wide bandwidth sampling of different input signals with minimal physical changes.
User-selectable input gains of X1 and X10; input impedance of 10 MΩ.	Makes one volt input ranges available; reduced errors due to high input loading.	Analyzing wide band communications signals from receiver outputs.
Simultaneous Sample-and-Hold (SSH)	Allows scanning up to four input channels at once.	High-speed cross-channel computation, beam-former coherency for sonar or acoustics, telemetry, multiple-carrier demodulation, and highly concurrent system testing.
FIFO data memory configuration.	Allows collection of 'seamless' wide-bandwidth samples of millions of samples or better.	Long baseline studies in astrophysics, stress life testing, and anomalous pattern searches.
Parallel digital data 'outport'	Lets external processors read data at high rates, eliminating bus delays.	Array processors, host mainframe I/O ports.
Software-programmable timers.	Allows precise control over conversions and multi-channel scans.	Software-programmable user-supplied Direct Memory Access (DMA) data transfers to host memory.
I/O status register and programmable interrupts.	Allows monitoring events from the host bus.	
Optional external trigger interrupt.	Allows precise synchronization with external events.	

FUNCTIONAL SPECIFICATIONS

Typical at +25 °C, gain = 1, dynamic conditions unless noted.

ANALOG INPUTS

	614A	614B, E	614C	614D
Full Scale Input Ranges				
Gain = 1, 0 to +5V	–	–	✓	–
0 to +10V	✓	✓	✓	–
±10V	✓	✓	✓	–
±5V	–	✓	✓	–
±1.25V	–	–	–	✓
Gain = 10 (Note 7)				
0 to ±1V	✓	–	–	–
±1V	✓	–	–	–

Number of Channels	4 Channels (Models A, B, C) 1 Channel (DVME-614D) 16S/8D Channels (DVME-614E)
Input Configuration	Single-ended, non-isolated (614A - D) Single-ended or differential (614E)
Input Impedance	10 Megohms (min.), power on *(See Tech. Note 1)* 50Ω in, 614D 1.5 Kilohms power off
Input Bias Current	±1 nA
Input Capacitance	10 pF per channel
Input Overvoltage	±15V max. (no damage)
Common Mode Volt. Range	±10V max. (614E)
Common Mode Rejection (Gain = 100)	80 dB (614E)
Overvoltage Recovery	2 Microseconds Maximum
Addressing Modes	a. Single channel b. Simultaneous Sample/Hold (614A) c. Sequential with autosequenced addressing d. Random addressing by host software

SAMPLE/HOLD CHARACTERISTICS

	614A	614B, E	614C	614D
Acquisition Time (max.) (10V step) to 0.01% of FSR	750 nS	750 nS	200 nS	50nS
Aperture Delay	6 nS	30 nS	30 nS	10nS
Aperture Delay Uncertainty	±1 nS	±5 nS	±5 nS	±10pS
SSH Channel-to-channel Linearity Tracking	±0.03%	–	–	–
Droop Rate, µV/µS	1	1	1	1

A/D CONVERTER

	614A	614B	614C, E	614D
Resolution	12 bits	14 bits	12 bits	12 bits
Conversion Period	500 nS	1 µS	1 µS	200nS

Output Coding	Positive-true right-justified straight binary (unipolar) or right-justified two's complement (bipolar) with sign extension through bit 15.
Trigger Sources (Software selectable)	a. Local Pacer sample clock b. External TTL sample clock c. Analog threshold comparator d. Host write to channel address register.

TOTAL SYSTEM DYNAMIC PERFORMANCE

	614A	614B	614C	614D, E
Full Scale Temp. Coef. LSB per °C	±0.1	±0.3	±0.1	±0.1
Zero or Offset Temp. Coef. LSB per °C	±0.1	±0.3	±0.1	±0.1
Integral Non-linearity, LSB	±1	±1.5	±1	±1
Diff. Non-linearity, LSB	±0.75	±1	±0.75	±1
Power Supply Rejection, (% of bus +5V)	±0.004	±0.004	±0.004	±0.004

A/D MEMORY

Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024 A/D samples, standard. Up to 4096 A/D samples (optional)

TOTAL SYSTEM DYNAMIC PERFORMANCE

See Tech. Note 2	614A	614B [614E]	614C	614D
System Bandwidth (single channel, half-scale input)	1 MHz	200 KHz	1 MHz	2.5 MHz
Total Throughput to FIFO (single channel, gain=1)	700 nS	2 µS	1µS	250 nS
Throughput to FIFO (sequential channels, gain = 1) (See Tech. Note 3)	1 µS	3 µS [4 µS]	2 µS	–
Throughput to FIFO (sequential channels, gain = 10)	10 µS	–	–	–
Total Harmonic Distortion, min. with half-scale input (See Tech. Note 4)	-72 dB	-75 dB [-72 dB]	-72 dB	-68dB
System Noise (referred to input)	200 microvolts, dc to 100 KHz			

TRIGGER CONTROL

Timer/Counter	82C54, (programmable)
Functions	a) A/D EOC sample count b) A/D start rate (16 bit divisor) c) Scan or frame rate (16 bit divisor)
Pacer Sample Counter	1 to 65.536 samples. Drives the Acquire flag/interrupt.
82C54 Clock Source (User-selectable)	a) Internal 8 MHz clock derived from VMEbus SYSCLK. b) External BNC TTL input, 10 MHz max.
Scan Clock Source	125, 250, or 500 KHz
Analog Trigger Input Range *(See Tech. Note 5)*	±10 Volts
Analog Trigger Response	2 microseconds to set status flag
Analog Trigger Hysteresis	40 millivolts

ANALOG OUTPUT

Number of Channels	One channel
Function	a) General purpose analog output
(user-selectable)	b) Threshold comparator for A/D trigger.
Resolution	12 bits
Output Voltage Range (User-selectable)	0 to +10V, ±5V, ±10V
Linearity	±0.05% of FSR
Settling time (10V step)	5 microseconds to 0.05%
Input Coding	Straight binary

VMEbus INTERFACE

Standards Compliance	IEEE P1014/D1.0
Data Bus Width	16 bits using P1 connector.
Address Bus	24 address lines (A23-A01) plus 6 Address Modifiers.
Address Modifier Codes	39 hex or 3D hex, selectable.
VMEbus Interrupt	1 line, selectable IRQ 1-7*. Asserts maskable programmable 8-bit vector ID code.
Architecture	SAD24:SD16 slave consisting of 16 contiguous word registers.
Bus Interrupt Sources	Scan acquire flag (sample count), FIFO full or half full.
Control/Status Functions	FIFO reset, FIFO flags, interrupt select and status, trigger source, timer control and period, sample count load, parallel outport transfer status, A/D enable, MUX autosequence.
Data Transfer	Uses 16 MHz VMEbus SYSCLK signal to generate DTACK* with selectable

PARALLEL PORT	
Parallel Outport	16 lines, TTL levels from FIFO. Includes ready out, acknowledge in and transfer enable in handshakes. Outport steering is software enabled.
Function	Asynchronous slave to remote master. Does not provide addressing. All data is sequential. The transfer enable input from a remote master is displayed as a status bit.
Parallel Port Loading	24 mA out, 1.6 mA in
Parallel Port Data Rate	4 MHz max. to external processor
CONNECTORS	
VMEbus, P1	96-pin male DIN connector. The P2 connector is not used.
Analog Input Connectors	Four BNC bayonet coaxial, mounted on front panel. DB-25 used for 614E
Multipurpose Connector	5th BNC user-selectable for: a) Pacer trigger input b) Analog threshold comparator input c) D/A output
Parallel Port	Front panel 25-pin DB-25S female. Provides external clock in.
MISCELLANEOUS	
Power Required	+5V dc ±5% at 3.0 Amps max. from VMEbus.
Operating Temp. Range	0 to +60 °C. Forced cooling is recommended.
Storage Temp. Range	-20 to +80 °C
Relative Humidity	10% to 90%, non-condensing.
Altitude	0 to 10,000 feet.
Outline Dimensions	Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233,5 x 160 x 15,24 mm).
Weight	17 ounces (482 grams)
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Adjustments	Offset and gain per channel for SSH on DVME-614A. A single offset and gain pot is provided on DVME-614B,C, D, E.

① (Programmable gain is selectable on 2 channels on the DVME-614A only)

TECHNICAL NOTES:

1. The input impedance of 10 Megohms minimum avoids attenuation errors from external input source resistance. For many applications, an external inline 50 ohm shunt, inserted adjacent to the front connectors, is recommended to reduce coaxial line reflections and standing wave errors.

2. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

3. The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels were scanned, the maximum sample rate on any one channel of the DVME-614C would be 2 µSec. x 4 chan. = 8 microseconds (125 KHz per channel).

TECHNICAL NOTES (Cont.)

4. THD test conditions are:

   1. Input frequency — 500 KHz (DVME-614A); 200 KHz (DVME-614B, E); 300 KHz (DVME-614C); 1 MHz (DVME-614D)
   2. Generator/filter THD is assumed to be -90 dB min.
   3. THD computed by FFT to 5th harmonic.

$$THD = 20 \times \log 10 \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}$$

   4. Inputs are half-scale. No channel advance.
   5. A/D trigger rate 1.5 MHz (DVME-614A), 500 KHz (DVME-614B,C,E), 4 MHz (DVME-614D).

5. For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10 Volts.

6. Allow 20 minutes warmup time to rated specifications for model DVME-614B.

7. The DVME-614E offers programmable gain from X1 to X100 selected by a precision gain resistor. Higher gains will have increased settling delay.

Simultaneous Sample/Hold

Four input signals are sampled at the same time using the DVME-614A's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired, they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors from conventional mux scanning.

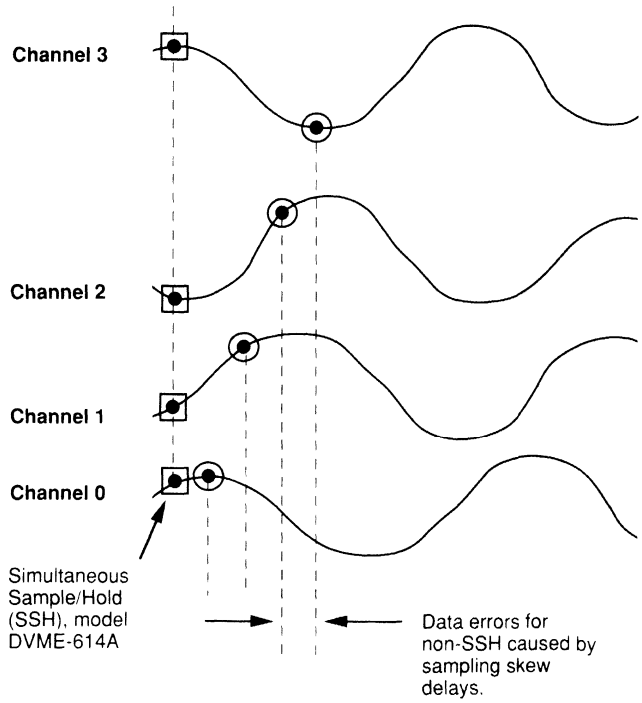


Figure 2. Advantage of DATEL's SSH Design

Register Memory Mapping

The Base address may be selected anywhere up to $FFFF00h on 32-byte boundaries.

Address (hex)	Direction	Description
Base + 0	Write	Command Register
Base + 0	Read	Status Register
Base + 2	Write	Channel Address Register
Base + 4	Write	D/A Data Register
Base + 6	Write	FIFO Reset Register
Base + 8	Not used	
Base + 0Ah	Not used	
Base + 0Ch	Read/Write	Interrupt Vector ID
Base + 0Eh	Read	FIFO A/D Data Register
Base + 10h	Read/Write	Counter #0 (82C54)
Base + 12h	Read/Write	Counter #1 (82C54)
Base + 14h	Read/Write	Counter #2 (82C54)
Base + 16h	Read/Write	Control Register (82C54)

At power-up or VMEbus reset, all registers contain zeroes except the FIFO HF and FF bits. The registers may be programmed in any sequence as long as the command register is last.

Command Register (Write BASE + 0)

15-8	7	6	5	4	3	2	1	0
x-x	Interrupt Source			Port/ Bus*	Trig Pol	Cnvrt Enbl	Trigger Source	
	FF	HF	ACQ					

"x" bits are not used or don't care.

Trigger Source [Bits 1,0]
- 00 =Scan by a write to the channel address register (normally not used).
- 01 =Scan by internal trigger.
- 10 =Scan by external TTL trigger.
- 11 =Scan by external analog threshold trigger.

Convert Enable [Bit 2]
- 0 =Disable A/D conversion (default)
- 1 =Enable A/D conversion

Trigger Polarity [Bit 3]
- 0 =Trigger on falling edge (default)
- 1 =Trigger on rising edge

Select FIFO Output Data Steering [Bit 4]
- 0 =Select VMEbus data register (Inhibit parallel port)
- 1 =Enable FIFO transfers to parallel port (Inhibit VMEbus data access)

Interrupt Source [Bits 7,6,5) These bits are OR'd.
- Bit 5 =Acquisition done flag (Counter 0 done)
- Bit 6 =FIFO half full flag
- Bit 7 =FIFO full flag
- 0 =Disable interrupt (default)
- 1 =Enable interrupt

(Only one interrupt source should be enabled at any one time.)

Status Register (Read BASE + 0)

15-8	7	6	5	4	3	2	1	0
x-x	FIFO Status			Ovr Smp Err	Xfr in Pro	Ana Trg Lvl	EOC Sts	ACQ Sts
	FF	HF	EF					

Acquisition Status [Bit 0]
- 0 = A/D scan not in progress or scan done (Counter 0 sample count was reached).
- 1 = A/D scan in progress (Counter 0 sample count not reached)

End of A/D Conversion Status (EOC) [Bit 1]
- 0 = A/D conversion in progress, data invalid
- 1 = A/D conversion done, data valid

Analog Trigger Comparator Output [Bit 2]
- 0 = Analog trigger input is below reference
- 1 = Analog trigger input is above reference

Transfer in Progress [Bit 3]
- 0 = Remote device not ready for transfer
- 1 = Remote device is ready for transfer

Bit 3 displays parallel inport pin 2 (external Transfer Enable In) AND'd with command bit 4.

Oversample Error [Bit 4]
- 0 = No error
- 1 = A/D triggered before EOC is done.

Bit 4 is cleared by disabling A/D conversions (write command 2=0).

FIFO Status Flags [Bits 7,6,5]
- Bit 5: 0=FIFO is empty, 1= FIFO not empty
- Bit 6: 0=FIFO is half full, 1=less than half full
- Bit 7: 0=FIFO is full, 1=FIFO is not full

Note the negative true coding on these bits.

Channel Address Register (Write BASE + 2)

15-8	7	6	5	4	3	2	1	0
x-x	Auto Incr	SSH Ctrl	Not Used		Channel Addr 3	2	1	0

Channel Address [Bits 3 -0]
- Only bits 1 and 0 are used for the 4-channel analog modules. 4 bits are used for DVME-614E.

Simultaneous Sample/Hold Control [Bit 6]
- 0 =Sequential or single channel mode
- 1 =Simultaneous sample/hold mode (see timing diagram)

In SSH mode, counter 0 must be programmed with the number of SSH channels (max = 4). One trigger is required per scan.

Channel Address Autoincrement [Bit 7]
- 0 =Single channel (no increment)
- 1 =Sequence channel address at start or end of A/D conversion

D/A Data Register (Write BASE + 4)

15-12	11	10	...	1	0
x-x	DA1 MSB	DA2		DA11	DA12 LSB

FIFO Reset Register (Write BASE + 6)

15	...	00
x		x

Any write to this register will clear the FIFO and set the empty flag true. If A/D conversion is still running, the FIFO will be not empty when the next A/D sample EOC occurs.

Interrupt Vector Register (Read/Write BASE + 0Ch)

15-8	7	6	5	4	3	2	1	0
x-x	V7	V6	V5	V4	V3	V2	V1	V0

This register may also be used to verify proper board addressing before interrupts are enabled. Write and read back a range of values into the bits 7 - 0.

FIFO Data Register (Read BASE + 0Eh)

15	14	13	12	11	...	00
S	S	S	S	MSB		LSB

12-bit A/D data

15	14	13	...	00
S	S	MSB		LSB

14-bit A/D data

"S" bits are sign-extended from either bit 11 (12 bit A/D's) or bit 13 (14-bit A/D's) in bipolar input range. For unipolar ranges, S = 0.

82C54 Programmable Interval Timer

The DVME-614 User Manual, shipped with the board, contains detailed programming information.

Counter Register (Read/Write BASE + 10h-Counter #0) (Read/Write BASE + 12h - Counter #1) (Read/Write BASE + 14h - Counter #2)

15-8	7	6	5	4	3	2	1	0
x-x	C07	C06	C05	C04	C03	C02	C01	C00

Control Word Register (Read/Write BASE + 16h)

15-8	7	6	5	4	3	2	1	0
x-x	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Select Counter	SC1	SC0	
	0	0	Select counter #0
	0	1	Select counter #1
	1	0	Select counter #2
	1	1	Read back command
Read/Load	RL1	RL0	
	0	0	Counter latch operation
	0	1	Read/Load LSB only
	1	0	Read/Load MSB only
	1	1	Read/Load LSB then MSB
Mode	M2	M1	M0
	x	1	0 Rate generation
	1	0	0 S/W trigger
	1	0	1 H/W trigger
BCD	BCD		
	0		16-bit binary count
	1		4-decade binary coded decimal count

Array Preprocessing

Figure 3 shows the DVME-614 installed in a typical VME application. The DVME-614 may be connected to an array processor board via a parallel port or the VMEbus. The parallel port offers higher speed by offloading block data transfers from the VMEbus. A separate cable is required for the parallel port.

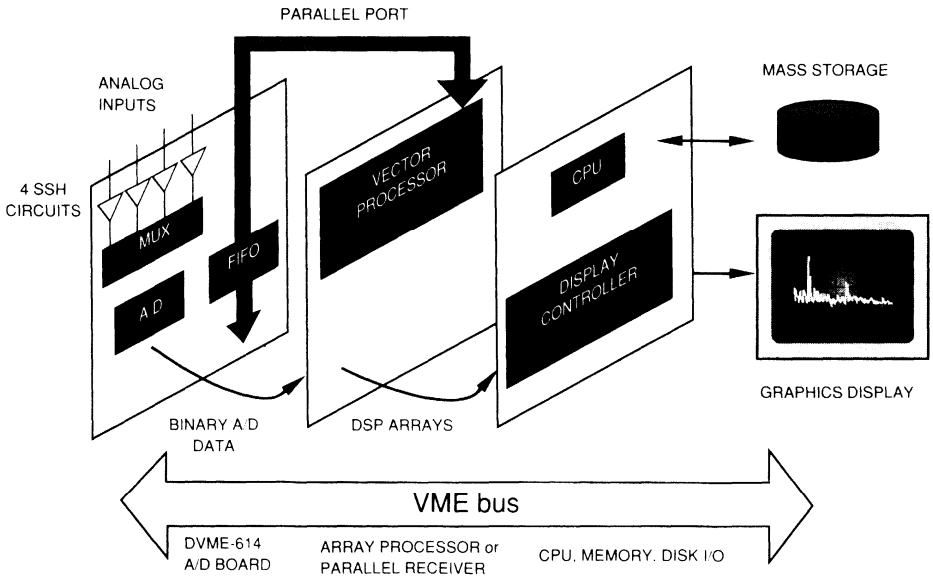
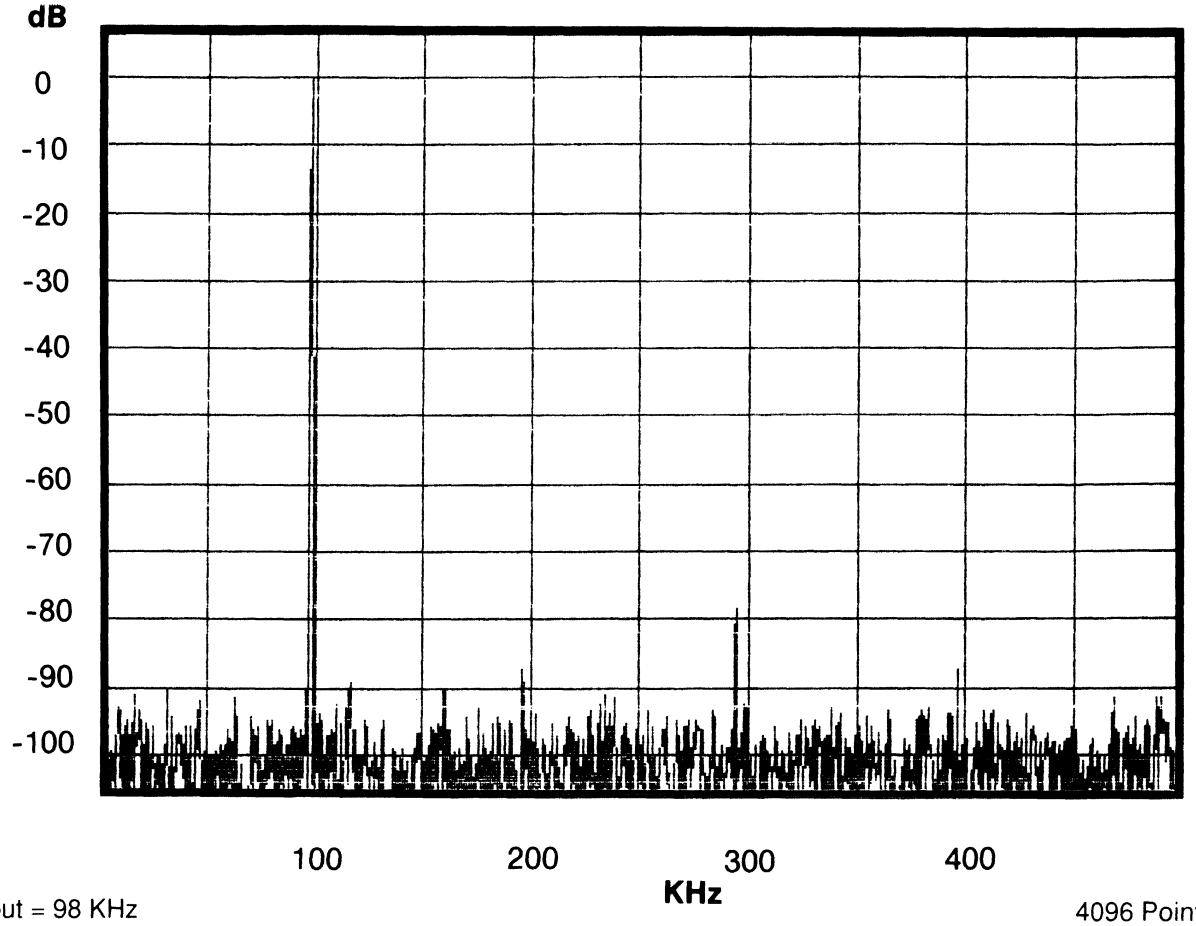


Figure 3. Array Pre-processing with the DVME-614



Input = 98 KHz
A/D Trigger = 1 MHz

4096 Points

Figure 4. DVME-614C Fast Fourier Transform

ANALOG TRIGGER

The analog threshold trigger is ideal for monitoring noisy inputs such as a telemetry receiver or RF/IF channel. As soon as the trigger threshold is transitioned, the FIFO immediately starts filling with A/D samples. The raw comparator output may be polled from the VMEbus in the status register, bit 2.

Since random noise may start this sampling process, the strategy is to collect a stream of A/D samples and quickly analyze if most of the samples contain valid data. If not, discard the sample array and start over.

The analog trigger input also accepts a purely digital input instead. By polling status bit 2, the analog trigger may be used as a general-purpose external control input. For example, this would terminate a high speed A/D file recording on disk from an external event

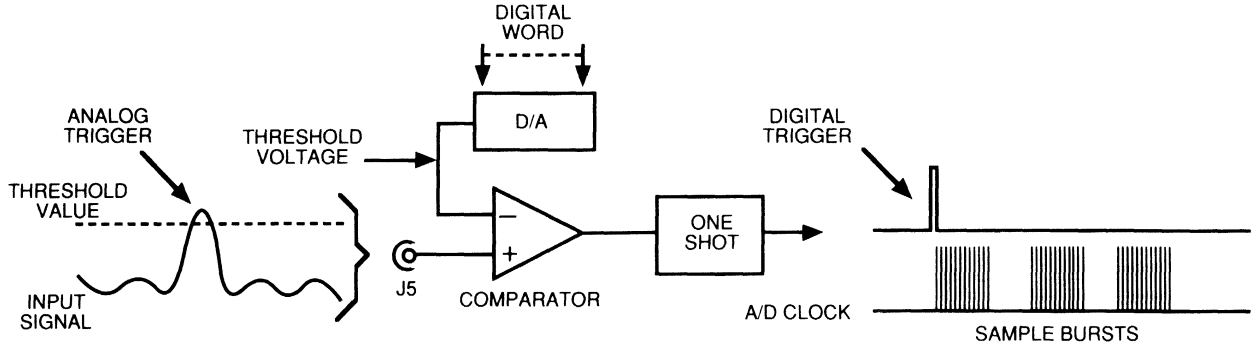


Figure 5. Analog Threshold Trigger

System Timing Diagram

Because of the flexibility of the local timing and trigger systems, the DVME-614 operates in many modes. Figure 6 shows multiple trigger configurations with the Acquire flag as an A/D converter clock gate. Triggering may be from internal or external clocks or from the analog comparator. For precise phase tracking, use both an external trigger and an external A/D start clock.

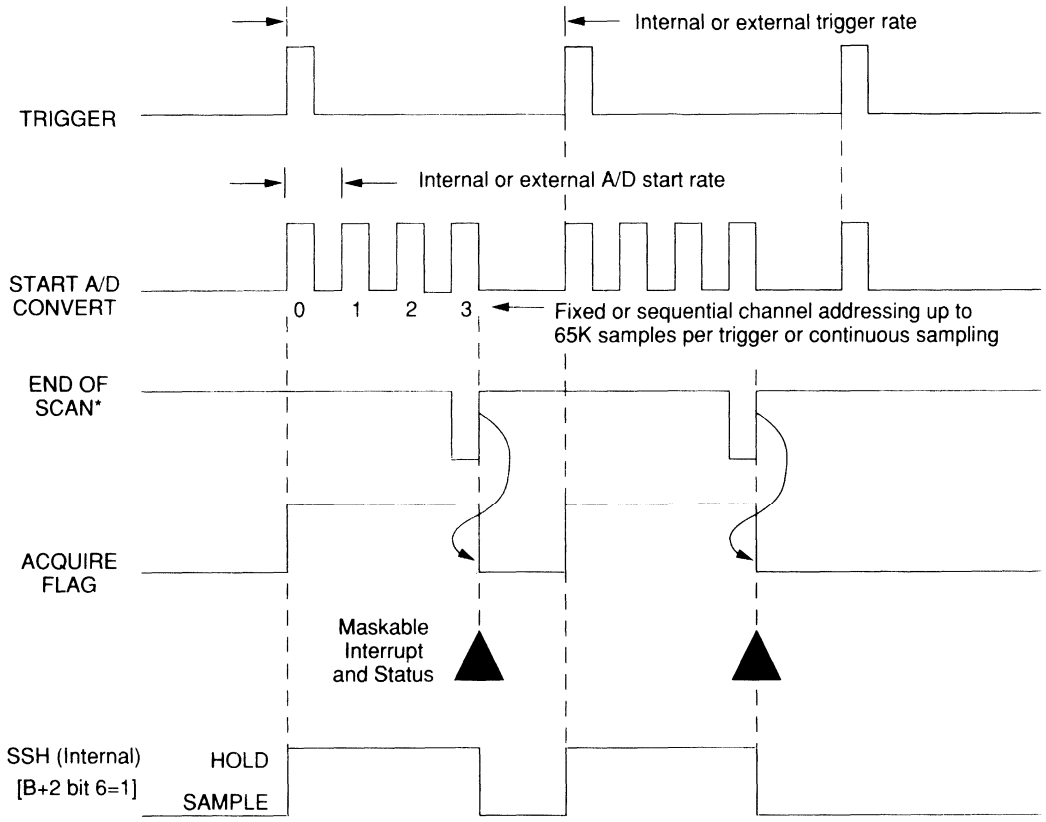


Figure 6. Trigger per Scan Mode

ORDERING GUIDE

Model	A/D Bits	No. of Channels	Single Channel Sample rate	FIFO size (A/D samples)	Simul. S/H	PGA
DVME-614A1	12	4	1.5 MHz	1024	4 channels	x1,x10
DVME-614A2	12	4	1.5 MHz	4096	4 channels	x1,x10
DVME-614B1	14	4	500 KHz	1024	none	none
DVME-614B2	14	4	500 KHz	4096	none	none
DVME-614C1	12	4	1 MHz	1024	none	none
DVME-614C2	12	4	1 MHz	4096	none	none
DVME-614D1	12	1	4 MHz	1024	none	none
DVME-614D2	12	1	4 MHz	4096	none	none
DVME-614E1	12	16S/8D	250 KHz	1024	none	1-100
DVME-614E2	12	16S/8D	(scan)	4096	none	1-100

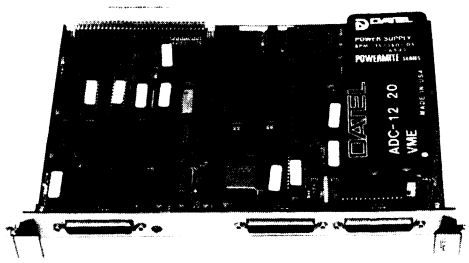
A software disk and user manual are included.
Boards are power-cycle burn-in tested.

DVME-691 Screw terminal signal conditioning panel, pin-compatible to DVME-614E

DVME-601 Series
16S or 8D-Channel 68010-based VME A/D Coprocessor Board

FEATURES

- **Local 8 MHz 68010 CPU plus:**
  - **— 64 Kb Private RAM**
  - **— 64/128 Kb EPROM**
  - **— 64 Kb Dual-ported RAM**
- **Various analog-to-digital front ends:**
  –12 Bits, 2,4, or 20 μSeconds
  –16 Bits, 35 μSeconds or 400 mSeconds



- **16 Single-ended or 8 differential on-board analog input channels expandable to 232 total channels using DATEL's slave MUX boards.**
- **Simultaneous A/D scanning and host transfer of previous scans. Ideal for DSP, FFT, ATE, graphics.**
- **Monitor/Executive firmware to run in "no program mode" or from user programs.**
- **RS-232-C serial port to debug optional user software. Programs may be downloaded through dual-port RAM or serial port and reprogrammed in EPROM.**
- **Programmable Peripheral I/O (68901):**
  - **— RS-232-C serial port USART.**
  - **— Three timer outputs which are software-programmable as interrupts, A/D start triggers, or pulses.**
  - **— Two 8-bit counter inputs.**
  - **— Five TTL I/O bits or interrupts.**
- **On-board +5V dc-to-dc power converter**
- **Programmable vectored interrupt.**
- **A/D Start by external trigger, timer or program.**
- **Sample-to-memory transfers at up to 300 KHz.**
- **Easily integrates with popular host multitasking Real Time Operating Systems such as UNIX, PDOS, OS-9, and VRTX.**

Today's VME environment requires that busy host processors run real-time operating systems, seriously affecting the host system's processing speed. DATEL'S DVME-601 coprocessor board integrates high-performance A/D data acquisition with a local 68010-based microcomputer. This unique single-board design lets the host handle other tasks while the DVME-601 smart A/D board simultaneously collects analog data.

GENERAL DESCRIPTION

Unlike dumb A/D boards, the DVME-601 coprocessor board automatically collects scanned data without delaying other host tasks. When A/D data is ready, the DVME-601 coprocessor board can interrupt the VME host. The host can then transfer data from previous scans to memory without halting collection of the next scan's data.

Typical applications for the DVME-601 include high-speed process control loops, analytical instruments, vehicular data recorders, ATE equipment and communications testers. The block-oriented, interrupt-controlled memory transfers of A/D scans to the host are particularly suited to digital signal processing applications. Such applications include acoustics, sonar, high-speed mapping, seismology, medical imaging, graphics, array processing, FFT's, and waveform analysis. Using the single-channel fast-throughput mode and the 4 μSec., 12-bit converter yields true speeds of up to 170,000 samples per second to memory (single channel, gain = 1).

As shown in Figure 1, the data acquisition section includes an analog input multiplexer with 16S/8D local channels expandable up to 232 total channels using DATEL's slave multiplexer boards. The board includes an instrumentation amplifier which may be resistor-programmed by the user for gains of up to 1000. A choice of pluggable A/D converter modules is offered on four different models. Resolution from 12 to 16 bits is available with 12-bit conversion speeds down to 2 μSec.

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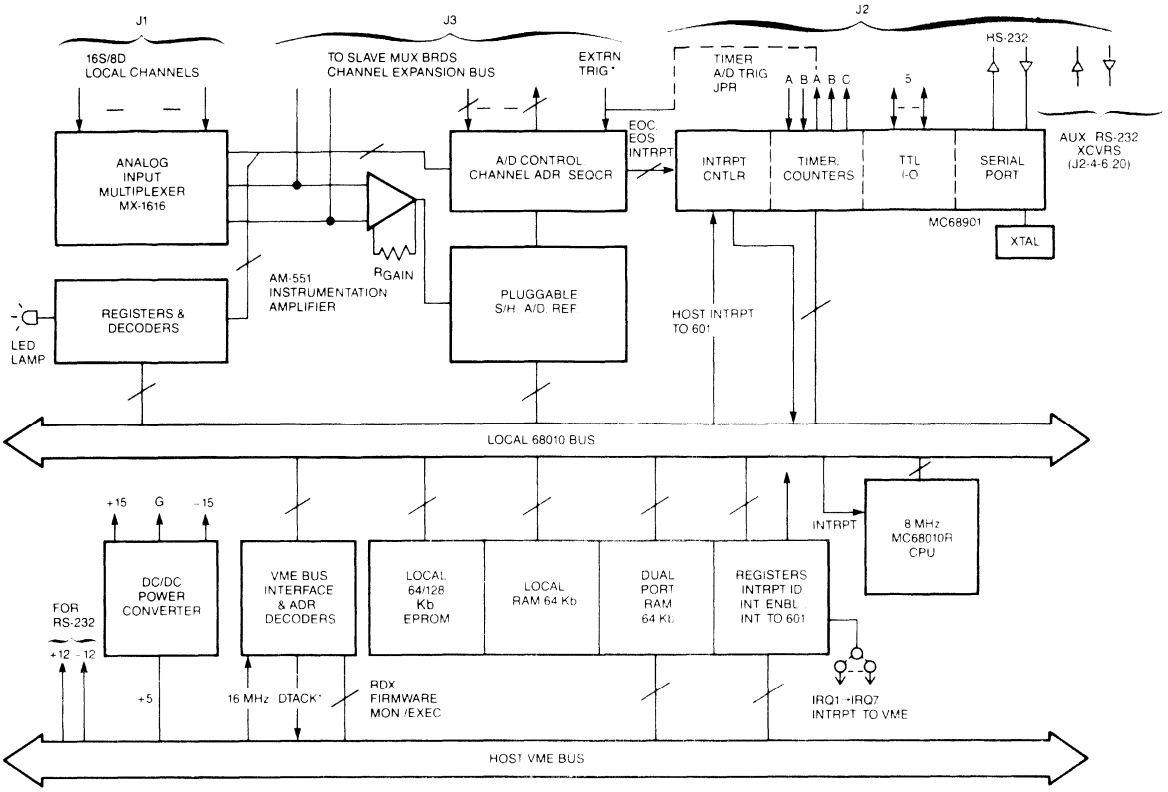


Figure 1. DVME-601 Coprocessor Board Simplified Block Diagram

External triggers, the internal programmable timer, local programs, or host commands may initiate A/D conversions. On-board EPROM firmware manages all of these start modes. A dc-to-dc converter supplies low-noise, regulated power to the data acquisition section.

The primary interface between the DVME-601 and its VME host is a 64 Kb dual-ported random access memory (DPR). The DPR is used for commands, subroutines and parameters, control/status bits, A/D data blocks, optional downloads of user programs, and bidirectional interrupts between the DVME-601 and the host. The maskable interrupt to the VMEbus normally occurs after A/D scanning, but may also be issued by a local user program.

Executive firmware included in the EPROM offers many ways to manage the DPR including swapped buffer ("ping-ponged") A/D scan transfers while the host reads the alternate buffer. The user may run the DVME-601 either in the "no-programming" mode or may load and execute their own programs. The no-program mode uses fast A/D routines supplied in the EPROM. The firmware also includes a serial port monitor program for developing optional user programs.

The DVME-601's full power and flexibility is realized with user-written software. As a high-performance, general-purpose microcomputer, the DVME-601 is ideal for automatic A/D data collection and arithmetic pre-processing of A/D data before sending it to the host. Transferring pre-processed results rather than raw data enhances total system performance while the host continues with disk, display, or control activities. Programs may be developed in the host, saved on disk, then downloaded to local RAM via the DPR or serial port. The pluggable EPROM may be reprogrammed by the user or by DATEL under special order. Any language may be used such as Assembly, BASIC, FORTRAN or C if it can be compiled to 68010 code.

The local microcomputer consists of an 8 MHz MC68010 microprocessor, 64 Kb of pluggable EPROM (socketed to 128 Kb), 64 Kb of DPR and 64 Kb of private RAM. Total local storage of A/D data may approach 62,000 samples using the DPR plus private RAM if no other program is using RAM space.

A programmable 68901 I/O peripheral controller is also included as part of the board design. This device offers an interrupt controller, an RS-232-C serial port, four timer/counters, and five I/O bits. Some of the timers and the serial port are used by the monitor/executive firmware but may be reprogrammed by the user to include external interrupts. A second RS-232-C serial port is available using a software UART and the I/O bits. A green front panel LED lamp lights to confirm power-up self-test and may be programmed by the user for alarms, etc.

Using only the serial port, a 16 MHz clock, and a +5V dc power supply, it is even possible to operate the DVME-601 in stand-alone mode, not connected to the VMEbus. Commands and A/D data pass through the port at rates of up to 19.2 Kb.

The board uses +5V dc at 2.8 A and ±12V dc at 2 mA (typical) from the VMEbus. Connections are made only to P1 (P2 is not used to assure compatibility with most hosts). Data transfer is 16 bits wide. The DVME-601 is a D16 A24 slave board using 24 address lines and 6 address modifier lines. The board occupies 64 Kb of host memory. A single interrupt to the host asserts a programmable interrupt vector. Three front panel D-type connectors provide physical interfacing for local analog inputs, analog slave-mux channel expansion, and for the serial/parallel/timer I/O.

The DVME-601 is a 9.19″W × 6.3″D × 0.6″H (233,5 × 160 × 15,2 mm) 6U board. It includes a comprehensive user's manual with programming information. Access to the EPROM source code in several formats is available to customers upon special request.

FUNCTIONAL SPECIFICATIONS
(Typical at +25°C, Gain=1, unless noted.)

DATA ACQUISITION SECTION

Number of On-board Channels . . . . 16 single-ended or 8 differential

Number of Off-board Channels . . . Up to 224 single-ended or 160 differential using DATEL's external channel multiplexer boards. (10 MUX brds. max.)

Total Addressable Channels . . . . . Up to 232 single-ended or differential

Input Voltage Range . . . . ±10 V full scale. (±5V, 0 to +10V, and 0 to +5V may also be available. See chart page 8.)

Common Mode Voltage Range . . . . . ± 10V, maximum, non-isolated

Common Mode Rejection (dc to 60 Hz, CMV = ±10V) . . . . . 80 dB, gain=1 with 1 KΩ source unbalance

Input Bias Current . . . . . ±200 pA

Overvoltage Protection . ±30V dc, maximum sustained

Input Impedance . . . . . Power on: 1000 MΩ, differential or to ground. Power off: 1.5 KΩ

A/D Output Coding (All models) . . . . . Bipolar 2's complement, or bipolar offset binary. The DVME-601A is jumperable for unipolar straight binary.

Instrumentation Amplifier Type and Gain Range . . . . . AM-551, supplied as gain = 1. May be resistor-programmed by user up to gain=1000 with increased settling delay.

Instrumentation Amplifier Settling Delay (gain = 1) . . . . . 3 μSec. to 0.01% of FSR

Adjustments . . . . . Instrumentation Amplifier offset, A/D offset and A/D gain.

LOCAL MICROCOMPUTER

CPU Type and Clock Speed . . . MC68010R8, 8 MHz (requires VMEbus SYSCLK)

Local Data Bus Width . . . 16 Bits

Local Read/Write Memory . . . . . 64 Kilobytes static RAM (no VMEbus access)

Local Read-only Memory . . . . . UV-erasable EPROM, 64 Kb supplied as two 27C256's but is socketed for two 27C512's totaling 128 Kb.

Dual-ported Read/Write Memory . . . . . 64 Kb (VMEbus and local access)

Front Panel LED Lamp . . Green LED lamp is lit if local CPU power-up self-test succeeds. User software may use the lamp for alarms, etc.

A/D-S/H RESOLUTION AND CONVERSION PERIOD OPTIONS
(See Technical Note 1)

Model	Resolution	Convert time	Thruput to RAM
DVME-601A	12 Bits	20 μSec.	40 KHz
DVME-601B	12 Bits	4 μSec.	100 KHz
DVME-601C	16 Bits	35 μSec.	25 KHz
DVME-601D	16 Bits	400 mSec.	2.5 Hz
DVME-601E	12 Bits	2 μSec.	see notes
DVME-601F	14 Bits	4 μSec.	100 KHz

SYSTEM PERFORMANCE

Specifications	A/D Type 601A 12 bit,	601E,B 12 bit,	601C 16 bit,	601D 16 bit,	601F 14 bit,
Speed	20 μS	2 or 4 μS	35 μS	400 mS	4 μS
Accuracy, min	0.025% of FSR	0.05% of FSR	0.01% of FSR	0.0063% of FSR	0.01% of FSR
Non-linearity & noise, max.	1/2 LSB	1/2 LSB	2 LSB	2 LSB	2 LSB
Zero Tempco max.	±20 ppm/°C	±20 ppm/°C	±20 ppm/°C	±10 ppm/°C	±15 ppm/°C
Gain Tempco max.	±20 ppm/°C	±20 ppm/°C	±20 ppm/°C	±10 ppm/°C	±15 ppm/°C

External A/D Start Trigger . . . . . Negative-going TTL input with 4.7 KΩ pullup to +5V. Pulse width is 100 nSec. minimum, 2 μSec. max.

Local Pacer Clock . . . . . Software-programmable to cause either an A/D scan start or a single conversion.

Pacer Clock Interval Range . . . . 3.255 μSec. to 41.667 mSec. using one timer.

Software Reset . . . . . Write to BASE + $FFF9, bit 0

PERIPHERAL I/O CONTROLLER

Controller Type . . . . . MC68901 multifunction peripheral, crystal-controlled, 2.4576 MHz, user-programmed.

Interrupts

Local Hardware Interrupts to 68010 CPU (Maskable) . . . . . A/D End of Conversion, A/D End of Scan, VMEbus host command request

Local Software Interrupts (Programmable) . . . . . Any timer count reached or I/O bits 0 through 4.

Digital I/O

Number of I/O Lines . . 5 lines, individually programmable as inputs, outputs, or interrupts.

Logic Levels . . . . . TTL levels, 1 load maximum with 10 KΩ pullups to +5V.

PERIPHERAL I/O CONTROLLER (cont.)

Timer/Counters

Number of Timers . . . . . 4 8-bit timers with pre-scale up to divide-by-200.

Timer Outputs . . . . . 3 outputs, (Timers A,B,C), 1 TTL load maximum. Timer D is the USART baud clock but may be reprogrammed.

Timer/Counter Inputs . . . 2 inputs, TTL levels with 10 KΩ pullups to +5V.

Serial Port (See Technical Note 2)

Number of Serial Ports . . 1 USART, full duplex, RS-232-C levels, DTE pinout.

RS-232-C Handshakes . . DTR, DSR, RTS, CTS programmed by the user. (See J2 pinout).

Modes . . . . . Synchronous or asynchronous.

Number of Stop Bits . . . . 0, 1, 1.5, or 2

Number of Data Bits . . . . 5, 6, 7, or 8

Parity . . . . . Odd, even, none for receiver. Transmitter is user-coded.

Baud Rates . . . . . Up to 19.2 Kilobaud.

VMEbus INTERFACE

Standards Compliance . . IEEE P1014/D1.0

Data Bus Width . . . . . 16 Bits

Address Bus . . . . . A24 D16 slave, 24 address lines (A23-A01) plus 6 address modifiers, jumper selected.

Address Modifier Codes . . . . . 39 hex or 3D hex, jumperable.

Architecture (See memory map) . . . . . Dual-ported 64 Kb block mapped on 64 Kb boundaries.

VME Bus Interrupter (See Note 3) . . . . 1 line, jumper-selectable IRQ1* through IRQ7*.

Data Transfer . . . . . 16 bits using P1. Generates DTACK* derived from 16 MHz bus clock.

CONNECTORS

VMEbus, P1 . . . . . 96-pin male DIN connector. P2 connector not used.

Local Analog Input, J1 . . 25-pin DB-25S female on front panel.

Multifunction I/O Peripheral (68901), J2 . . . . . 25-pin DB-25S female on front panel.

Analog Input Channel Expansion Bus, J3 . . . 25-pin DB-25S female on front panel, compatible to DATEL DVME-64X series multiplexer boards.

MISCELLANEOUS

Power Required . . . . . +5V dc ±5% at 3.1 A max. and ±12V dc at 10 mA max. from VMEbus for serial port. A local ±15V dc-to-dc converter is included for linear circuits

Operating Temperature . . . . . 0 to +60°C

Storage Temperature . . . −20°C to +80°C

Relative Humidity . . . . . 10% to 90%, non-condensing.

Outline Dimensions . . . . Double-height VME, 6U outline. 9.19″ W × 6.3″ D × 0.6″ H, (233,5 × 160 × 15,24 mm).

Weight . . . . . 17 ounces (482 grams)

TECHNICAL NOTES

1. The typical throughput rate is an aggregate time within a multichannel scan and does not include subroutine setup time. The rate includes times for channel sequencing, MUX, Inst. Ampl., S/H acquisition/settling, A/D conversion, and 68010 software times. The polled EOC STSNSC subroutine is used, triggering A/D conversion on each data read. Higher single-channel speed is available using the "fast-throughput" mode (delayed DTACK*). The DVME-601E offers 300 KHz in a long burst to local RAM, single channel, gain = 1. In multichannel, all modes require at least 6 microseconds (gain = 1) from channel sequencing to A/D start plus the A/D conversion time. Data transfer time may overlap A/D conversion.
2. EPROM Monitor firmware uses Timer D and the serial port. Communications format is 9600 baud, 8 data bits, no parity, and 1 stop bit. A 4800-baud software UART is formed with I/O bit 0 for optional serial S record downloads. Firmware also uses Timer A as an A/D start clock. The user may re-program all functions.
3. Asserts one interrupt ID code which is programmable from the host. A DVME-601 local register generates the interrupt. The host may mask this interrupt by writing to a DVME-601 DPR register.
4. For model DVME-601F, allow 20 minutes warmup to rated specifications.

DVME-601 FIRMWARE OVERVIEW

Memory Mapping

Table 1 shows the relationship between the local DVME-601 memory and the host DPR window. Arbitration circuits prevent simultaneous access to the DPR by delaying either the local DVME-601 DTACK* or the VMEbus DTACK*. Three addresses in the DPR are hardware-mapped from the host. They enable interrupts to the host, select the interrupt ID vector that is asserted and force a local 68010 interrupt to execute a Function Block Command or local subroutine.

A portion of the top of Read/Write DPR is reserved for control/status bits defined by the DVME-601 firmware. A portion of the local RAM is reserved for the DVME-601 system control, vectors and stacks. Data acquisition and 68901 registers, as well as a register to interrupt the host from a local program, are hardware-mapped in local memory.

Table 1. DVME-601 Memory Map

Local Memory		Host Memory	
$000000- $01FFFF	64/128 Kb Local EPROM (READ only)		
$020000- $02FFFF	64 Kb Local RAM (READ/WRITE)		
$040000- $04FFF7	64 Kb Shared Dual Port RAM (READ/WRITE)	Base + $0000- Base + $FFF7 [$FFF0-FFF7 are soft-mapped R/W cmd/stat. See manual]	Shared 64 Kb DPR (RD/WR)
$04FFF8 $04FFF9	Not used Not used	Base + $FFF8 Base + $FFF9	Enable interrupt to VMEbus (RD/WR) (Bit 7)
$04FFFA $04FFFB	Not used Not used	Base + $FFFA Base + $FFFB	Host interrupt ID Vector (RD/WR)
$04FFFC $04FFFD	Not used Not used	Base + $FFFC Base + $FFFD	Force command interrupt to DVME-601 (WR-only word from host)
$04FFFE $04FFFF	Not used Not used	Base + $FFFE Base + $FFFF	Not used Not used
$06XXXX	A/D Start Channel Address Reg. (WR)	Notes:	
$08XXXX	A/D Final Channel Address Reg. (WR)	1. Unlisted addresses are redundant or not defined. All addresses are in hexadecimal. "XXXX" bytes are not decoded and are don't care. Factory-jumpered base addressing is $FA0000.	
$0AXXXX	Command/Status Reg. (R/W) [EOC,EOS, LED, A/D, etc.]	2. Hardware registers from $6XXXX to $10XXXX require MOVE.W instructions. Local RAM from about $20000-21000 is reserved. 68901 registers require MOVE.B instructions or Read-Modify-Write.	
$0CXXXX	Start A/D Convert (WRITE only)	3. BASE + $FFFC is write-only from VMEbus and should be located beyond power-up memory testing.	
$0EXXXX	Force interrupt to VMEbus Host (WR)		
$10XXXX	A/D Data Register (READ only)	4. Software Reset is available at B + $FFF9, bit 0	
$120000- $12002F	68901 Intrpt/Timers/ USART/Parallel Port (READ/WRITE)		

A/D Converter Command Modes

Location $0AXXXX in the DVME-601's local memory map contains a command register. The settings of individual bits in this register determine:

- A/D converter triggering,
- modes of channel sequencing, and
- how the converter transfers data.

Executive firmware manages this register; however, it may be directly controlled by user-written programs as well. The addresses below refer to the local 68010 memory map (see Table 1). The command register controls the following hardware functions:

1. A/D conversion starts with a short settling delay before the actual conversion. Three events can trigger the delay:
   A. An external TTL trigger or timer input arrives. (The logic enables the trigger and waits for the falling edge.)
   B. The local CPU reads the A/D data register ($10XXXX).
   C. A write to location $0CXXXX occurs.

These modes may be partially combined. All modes must test the End of Conversion (EOC) bit to confirm that data is ready.

2. The start pulse may start either a single conversion or a scan of N channels as defined by the start and final channel address registers ($06XXXX and $08XXXX). If the start defines a SCAN, then individual samples must still be started by reading the A/D data register.
3. A "fast throughput" mode is offered where the A/D converter logic holds off the local DTACK* input to the 68010 until the End of Conversion output. This mode offers higher speeds by eliminating EOC polling. When used with a block move instruction loop which auto-increments the destination pointer, this acts like a DMA transfer. During DMA transfers, the instruction remains in the 68010's queue and requires no opcode fetch cycle.
4. A "re-scan mode" is offered which automatically reloads the start channel register when the End of Scan is reached. This mode yields higher speeds for repeated scans by eliminating the address register write.
5. The channel address sequencer may be inhibited from incrementing after each sample. This would be used for very high-speed single channel applications and is similar to loading the same address in both the start and final addresses registers.
6. The A/D start logic may be inhibited by local 68010 command. This would be used to ignore external triggers until ready or for other usage.

NOTE

EOC/EOS interrupts are always sent to the local 68901 interrupt controller but are normally masked off by programming the 68901 registers.

EPROM Firmware

The 64 Kb EPROM includes Monitor and Executive software. The Monitor helps in developing and debugging optional user-written programs and is available only via the RS-232-C serial port. This port is on the DVME-601's front panel J2 connector. The user simply connects a "dumb" terminal to this connector.

The Monitor is not required if the user chooses to control the DVME-601 only from the DPR using the Executive. After successful power-up testing, the LED is lit and the DVME-601 automatically enters the Monitor. This LED illuminates to indicate successful memory and I/O tests. The DVME-601 attempts to run the Monitor even if self-test fails. The Executive will be off, insuring that the DVME-601 will ignore any power-up bus activity in the DPR. The user switches the board from the Monitor to the Executive state via either the serial port or the DPR.

The Executive accepts function blocks loaded from the DPR by the host. The blocks may contain reserved command words, local subroutine addresses, and optional input or output parameters. The host tells the DVME-601 to execute a previously loaded command by writing to a reserved location in the DPR. This forces a local 68010 interrupt to branch to the command or routine.

A typical subroutine would set the start and final analog channel address registers. It would include these addresses as long-word parameters in a sequential list after the subroutine memory address. Another subroutine would start A/D scanning. Its "output parameter" would be blocks of digitized A/D data transferred to the DPR.

Subroutine addresses may also include the addresses of user-written code which was previously downloaded into local memory or reprogrammed in the EPROM. A function command is reserved to perform the DPR download of S records. Since the S records contain destination addresses and may be of any length, the code may be sent anywhere in usable local RAM. It can overlay previous code and can be repeated indefinitely at high speed. It can include tables as well as executable binary image since it is not executed as part of the download.

All of this activity is controlled by VMEbus commands via the Executive. While a subroutine runs, a reserved control/status area of DPR indicates when command execution is in progress

and when a command block is done. Any subroutine (including a long multiple A/D scan) may be interrupted to return to the command level or execute a different routine. Thus, the user has an extremely powerful, general purpose means of controlling the DVME-601.

Monitor Commands

A conventional hexadecimal firmware Monitor allows full access to the 68010 CPU registers, data acquisition registers, the 68901 peripheral, and to memory locations (including the DPR). Programs may be run under breakpoint and/or trace control. The Monitor also includes several A/D diagnostic commands to aid in calibration or hardware troubleshooting. A list of monitor command functions appears in Table 2.

Table 2. Summary of Monitor Command Functions

Monitor Commands
Read/Write CPU or memory registers
Display memory block in hexadecimal and ASCII.
Fill memory block with a constant.
Set or display breakpoint.
Trace one or more instructions.
Start execution until optional breakpoint.
Turn Executive ON or OFF (enable/disable DPR commands).
Transition to/from Executive or Monitor.
Auxiliary serial port download.
Start A/D sampling to serial port.

Executive Commands

The Executive accepts commands and optional parameters through the DPR. A major benefit of the Executive is a uniform sequential list method of passing subroutine parameters. User programs may also use this syntax or may develop their own parameter-passing method in another part of the DPR. If the user's serial port terminal is connected, the execution of Executive Function Blocks may be analyzed at the Monitor level. The Executive also traps non-executable subroutine addresses by performing a soft reset.

Executive Commands
Select the memory destination address of A/D scans as either local RAM, single DPR or swapped DPR buffers.
Select the source of A/D start triggers as external TTL, local timer, last A/D read or host command.
Select A/D triggering per conversion or per scan.
Select channel address sequencer to increment or not after each conversion.
Select start/final sequential channel addresses.
Select timer channel, period and control.
Transfer A/D scans from local RAM to DPR (after data pre-processing by a user-downloaded program).
Define whether scan transfers will wait for host Ready status or transfer without waiting.
Select how scanning will stop (N samples, N scans, buffer full, stop by host).
Download S records via DPR or auxiliary serial port and flag checksum errors but do not start execution.
Load subroutine addresses or function command block with optional parameter list and await execution.
Execute previously loaded commands or subroutine(s)
Memory block transfer.

The Executive allows for repeating or alternating blocks of sequential subroutines. They may be selected once, N number of times, or until stopped by the host. The DPR Download is one of the Executive commands. Most of the subroutines available through the Executive manage the data acquisition section. Table 3 lists the functions of executive commands available.

Speed by Architecture

The primary difference between the DVME-601 smart A/D board and "dumb" A/D boards is the increased total system throughput achieved by offloading the host. This is a result of simultaneous A/D scanning and concurrent host processing, plus using the DPR as a programmable buffer. Even greater system bandwidth may be possible by having the DVME-601 do arithmetic pre-processing of A/D blocks, delivering final results rather than raw input data.

Figure 2 shows the wasted idle times in the host for dumb A/D boards because an interrupt, polling, or DTACK* delay must occur with each sample.

The interrupt processing takes many microseconds to save stacks and registers and arbitrate with the Real Time Operating System. To realize the full speed of a dumb board, the host must be fully dedicated to data acquisition, leaving no time for non-A/D tasks. With fast converters and high bandwidth inputs, the short sample intervals make it inefficient to run the host in an interrupt mode, thereby locking out other host software tasks during data acquisition. The typical lack of memory on dumb boards for sample storage also means that the last sample is saved in the A/D converter and new sampling cannot start until the old sample is read.

The DVME-601 efficiently runs long blocks of thousands of samples, allowing ample time for host disk and display activity between blocks.

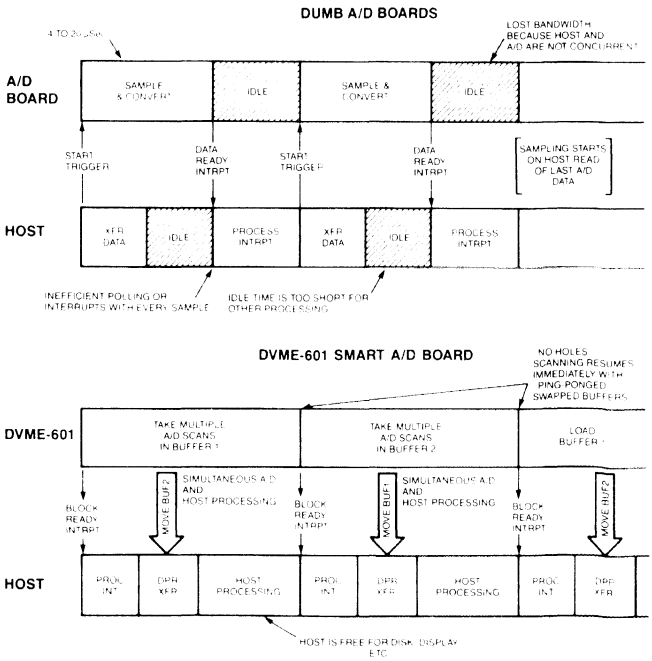


Figure 2. Speed by Architecture

I/O SIGNALS AND CONNECTIONS

A/D Channel Expansion Bus

(Please refer to the Channel Address Map, Table 4)

The DVME-601's J3 front panel connector accepts a flat cable assembly, such as DATEL Part Numbers DVME-C-01 or DVME-C-02, to form a channel expansion bus. The cable assembly plugs into DATEL's slave multiplexer boards installed in slots adjacent to the DVME-601 or in a nearby VME chassis. Available DATEL channel expansion boards include:

- DVME-641 A 32 Single-ended/16 Differential channel high-speed MUX;
- DVME-643 An 8 Differential channel low-level isolated MUX (for sensors such as thermocouples, RTD's, 4-20 mA loops, etc.); and,
- DVME-645 A 16 Single-ended/8 Differential channel simultaneous sample/hold MUX.

The DVME-645 is especially suited to array processing and DSP applications. This channel expansion bus allows the DVME-601 to directly control each slave MUX board and carries three classes of signals. They are:

1. Eight-bit channel address outputs from the DVME-601's address register, offering up to 256 total channels. This autosequencing register is software-controlled by the user's host program or DVME-601 firmware.
2. Buffered high-level switched differential analog signals into the DVME-601's instrumentation amplifier.
3. Control and handshake lines, an external A/D start trigger, and grounds.

Channel addresses are distributed to all MUX boards along the bus. The first 8 or 16 addresses are for local DVME-601 channels. Address selection logic and base address switches on each MUX board allows it to respond to a range of addresses. All other de-selected boards disconnect their analog outputs from the bus until addressed. For diagnostics, each MUX board has a LED lamp which turns on when that board is addressed. DATEL offers 2- and 3-connector cables to connect one or two slave MUX boards and users may fabricate flat cables for connecting up to 10 boards.

One of the control lines on the expansion bus is a TTL-compatible, open-collector A/D trigger. This lets the DVME-601's A/D start input be initiated from the trigger input on any multiplexer board. A single external event hardware trigger will start either one A/D sample and host interrupt or a scan of channels and interrupt on one or more boards. Alternatively, automatic channel sequencing and A/D conversion may be started from a DVME-601 timer by jumpering the timer output to the trigger input on the J3 connector. Software commands from the host will also start the A/D conversion process.

A settling delay control line output from each MUX board will delay the actual A/D conversion to synchronize settling times of low-level pre-amplifiers on the MUX slave boards. Through appropriate host A/D software, board addressing and input range selection, it is even possible to mix high- and low-level expansion input boards on the same bus.

Figure 3 shows how a DVME-601 Coprocessor board physically links to DATEL's slave multiplexer boards and field equipment.

Table 4. Analog Channel Expansion Address Map

Unused addresses	($FFh)
Expansion MUX Board N ⋮ Expansion MUX Board 2	
Expansion MUX Board 1	($0Fh or $1Fh)
DVME-601 16S/8D Channels	($00)

Input/Output Connections

Figures 4, 5, and 6 show the signals present on the DVME-601's J1, J2, and J3 connectors respectively. The connectors are dedicated as follows:

J1 Local Analog Inputs
J2 Multifunction Peripheral I/O Signals
J3 Analog Channel Expansion Bus

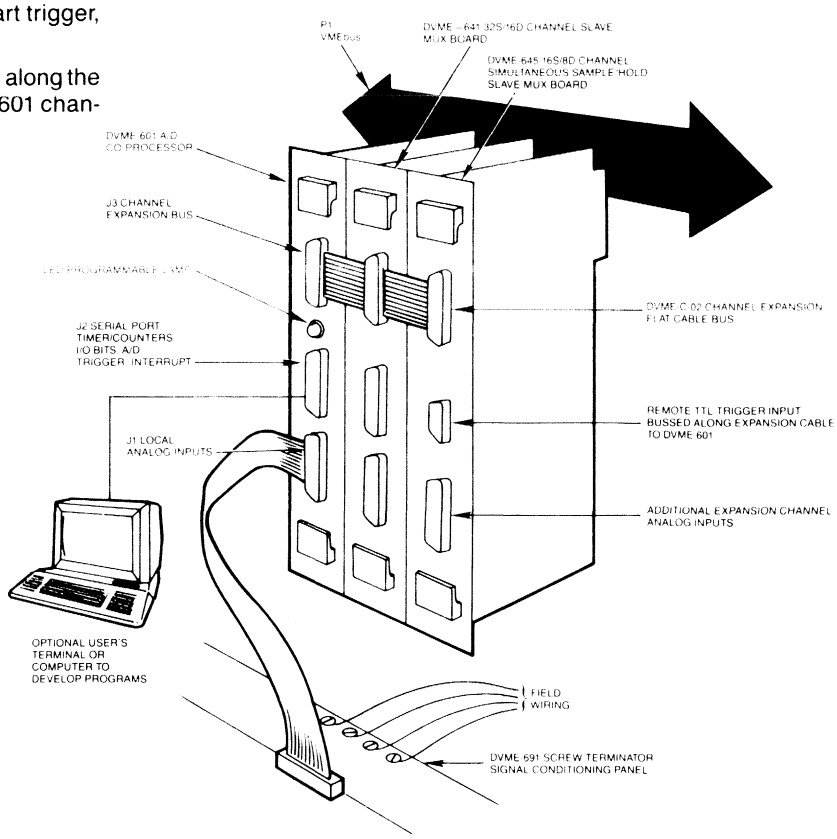


Figure 3. Front Panel Cabling and Wiring Connections

J1 (VIEWED FROM FRONT OF BOARD)

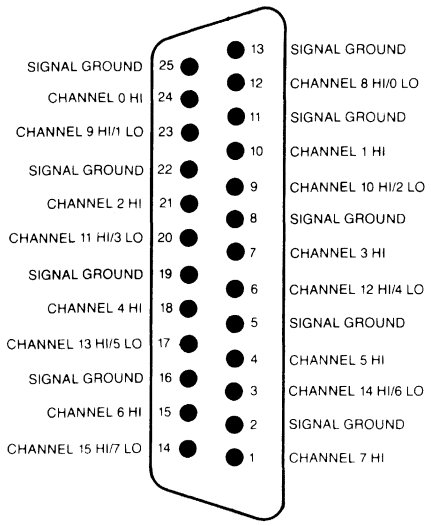


Figure 4. Local Analog Input Connector Analog (J1)

J2 (VIEWED FROM FRONT OF BOARD)

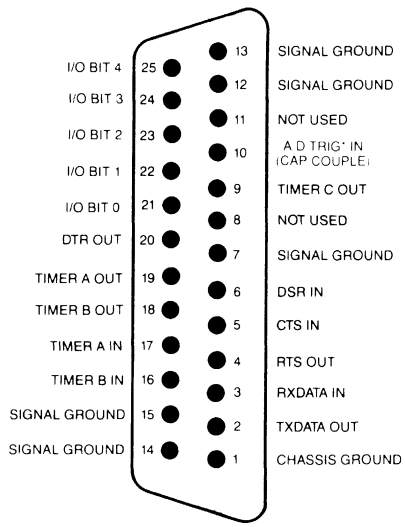


Figure 5. Multifunction Peripheral I/O Connector (J2)

J3 (VIEWED FROM FRONT OF BOARD)

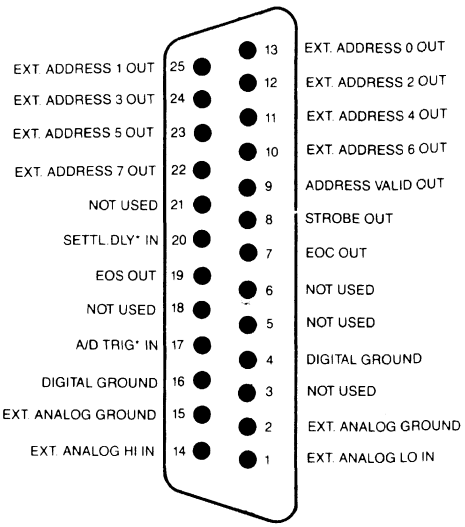


Figure 6. Analog Channel Expansion Bus Connector (J3)

ORDERING GUIDE

Model Number	A/D Bits, Conversion Speed, and Input Configuration
DVME-601A	12 Bits, 20 µSec., unipolar or bipolar
DVME-601B	12 Bits, 4 µSec., unipolar or bipolar
DVME-601C	16 Bits, 35 µSec., bipolar
DVME-601D	16 Bits, 400 ms, bipolar
DVME-601E	12 Bits, 2 µSec., unipolar or bipolar
DVME-601F	14 Bits, 4 µSec., ±10V

All models include a 64 Kb EPROM with Monitor/Executive firmware, a User's Manual, and a software disk. A substantial amount of unused EPROM is available to the user. DATEL will review custom software requirements under special order.

HARDWARE ACCESSORIES

Part Number	Description
DVME-691A	Rack-mount screw terminator panel with signal conditioning pads for 32S/16D input channels. Includes flat signal cables compatible with the DVME-601.
DVME-C-01	Channel expansion flat cable with 2 DB-25P connectors for use with one slave MUX board.
DVME-C-02	Channel expansion flat cable with 3 DB-25P connectors for use with two slave MUX boards.

CHANNEL EXPANSION SLAVE MUX BOARDS

Part Number	Description
DVME-641	32S/16D Channel high speed, high-level non-isolated MUX board.
DVME-643	8D Channel low-level, isolated MUX board.
DVME-645	16S/8D Channel simultaneous sampling MUX board.

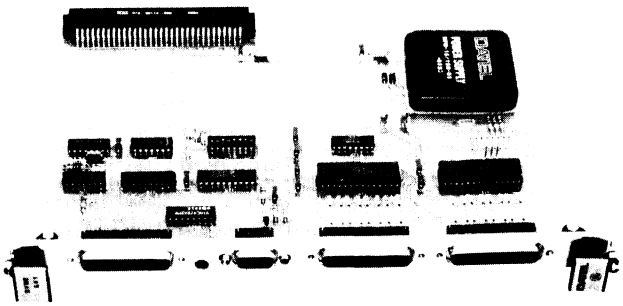
Contact DATEL for additional DVME-601 software on disk.

Input Range	Model DVME-601A	DVME-601E,B	DVME-601C	DVME-601D	DVME-601F
0 to +5V	X				
0 to +10V	X	X			
±5V	X		X		
±10V	X	X	X	X	X

DVME-641
32-Channel High-Level, VMEbus Expansion Board

FEATURES

- **Accepts 32 single-ended/16 differential expansion channels**
- **Directly accepts high-level inputs**
- **Hardware compatible with VMEbus specifications**
- **Interfaces to DATEL's DVME-601/611/612 A/D boards**
- **6 Microseconds settling time**
- **0.01% Full-scale range accuracy**
- **Low-cost**
- **Cascadable to up to 256 channels**
- **Includes a board selection LED lamp**



THE DVME-641 OFFERS CHANNEL EXPANSION TO DATEL's DVME-601/611/612 SERIES OF A/D BOARDS. THE CHANNEL EXPANSION BOARD IS DESIGNED TO ACCEPT HIGH-LEVEL INPUTS FROM UP TO 32 SINGLE-ENDED OR 16 DIFFERENTIAL INPUT CHANNELS. THE DVME-641 DRAWS POWER FROM THE VMEbus P1 CONNECTOR AND FITS INTO VMEbus CARD CAGES.

GENERAL DESCRIPTION

The DVME-641 is a low-cost channel expansion board that interfaces directly to DATEL's DVME-601/611/612 high-performance A/D boards. The board externally multiplexes up to 32 single-ended or 16 differential high-level input channels. The channel expansion board fits into a typical VMEbus host system. The DVME-641 is specifically useful for applications involving multiple-channel data acquisition or controlling numerous discrete process control loops. The low cost per channel makes the board ideal for most applications.

Figure 1 shows a typical multi-channel application for data acquisition from different types of inputs. In this application the host system selects the expansion channel on the DVME-641, DVME-643 or DVME-645 through the DVME-601/611/612 A/D board. The DVME-601/611/612 digital data is available on the VMEbus data lines for host system access.

ORDERING INFORMATION

DVME-641	32S/16D MUX board

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).

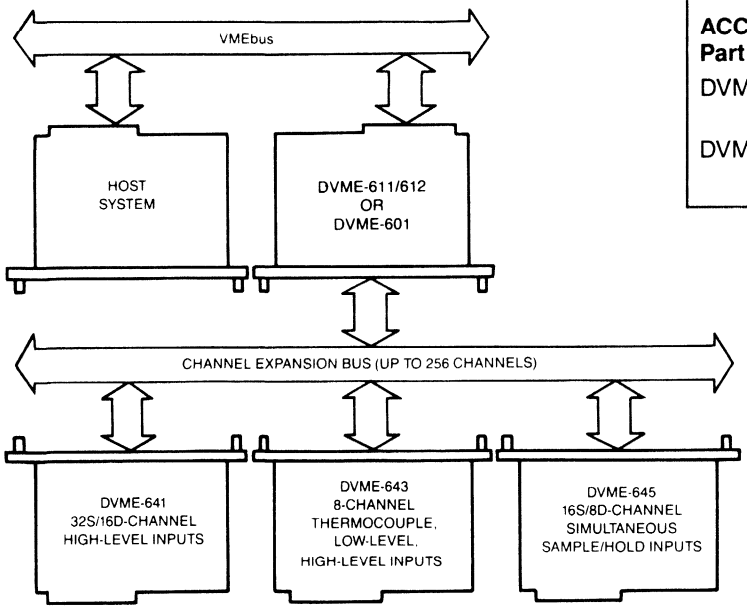


Figure 1: DVME-641 Application Configuration

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C unless otherwise noted)

ANALOG INPUT

Number of Channels	32S/16D
Channel Expansion	256S/256D*
Input Configuration	Single-ended or Differential
Input Range	± 10V dc
Analog Output	Differential
Interface	Analog Expansion Bus for DVME-601/611/612 boards
Common Mode Voltage (Specified for differential configuration only)	±10V dc, maximum non-isolated
Overvoltage Protection	± 35V dc, maximum
Off-Channel Leakage current	0.03 nanoamperes, typical 60 nanoamperes, maximum
On-Channel Leakage Current	0.1 nanoamperes,typical 300 nanoamperes, maximum
Output Settling Time (0 to 10V step input, channel-to-channel settling)	6 μseconds, maximum to rated accuracy
Full-scale Range Accuracy	0.01%, maximum
Output Impedance	2.5 Kohms, maximum

*Up to 10 slave MUX boards may be driven from one A/D master board at derated settling.

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector	96-pin male DIN connector
Analog Input - J1,J2 Connectors	Two 25-pin D-type DB-25S female connectors
External Trigger - J3 Connector	9-pin D-type DB-9S female connector
Analog Expansion - J4 Connector	25-pin D-type DB-25S female connector

POWER SUPPLY REQUIRMENTS

+5V dc ±0.5% at 0.4A typical, 0.6A maximum from P1 VMEbus connector

PHYSICAL CHARACTERISTICS

Outline Dimensions	9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)
Weight	11 oz. (311.85 grams)
Operating Temperature Range	0 to +60 °C
Storage Temperature Range	-20 to +80 °C
Relative Humidity	0 to 90% non-condensing

I/O CONNECTIONS

The DVME-641 uses J1, J2, J3, and J4 for analog input, external trigger, and channels expansion connections. Tables 1,2, 3, and 4 list these signals. VMEbus IACK and bus grant signals are daisy-chained.

Table 1: DVME-641 Analog Input Connector (J1)

PIN #	Single-ended	Differential
24	Channel 0 IN	Channel 0 High IN
12	Channel 16 IN	Channel 0 Low IN
25	Analog Return	Analog Return
10	Channel 1 IN	Channel 1 High IN
23	Channel 17 IN	Channel 1 Low IN
11	Analog Return	Analog Return
21	Channel 2 IN	Channel 2 High IN
9	Channel 18 IN	Channel 2 Low IN
22	Analog Return	Analog Return
7	Channel 3 IN	Channel 3 High IN
20	Channel 19 IN	Channel 3 Low IN
8	Analog Return	Analog Return
18	Channel 4 IN	Channel 4 High IN
6	Channel 20 IN	Channel 4 Low IN
19	Analog Return	Analog Return
4	Channel 5 IN	Channel 5 High IN
17	Channel 21 IN	Channel 5 Low IN
5	Analog Return	Analog Return
15	Channel 6 IN	Channel 6 High IN
3	Channel 22 IN	Channel 6 Low IN
16	Analog Return	Analog Return
1	Channel 7 IN	Channel 7 High IN
14	Channel 23 IN	Channel 7 Low IN
2	Analog Return	Analog Return

Table 2: DVME-641 Analog Input Connector (J2)

PIN #	Single-ended	Differential
24	Channel 8 IN	Channel 8 High IN
12	Channel 24 IN	Channel 8 Low IN
25	Analog Return	Analog Return
10	Channel 9 IN	Channel 9 High IN
23	Channel 25 IN	Channel 9 Low IN
11	Analog Return	Analog Return
21	Channel 10 IN	Channel 10 High IN
9	Channel 26 IN	Channel 10 Low IN
22	Analog Return	Analog Return
7	Channel 11 IN	Channel 11 High IN
20	Channel 27 IN	Channel 11 Low IN
8	Analog Return	Analog Return
18	Channel 12 IN	Channel 12 High IN
6	Channel 28 IN	Channel 12 Low IN
19	Analog Return	Analog Return
4	Channel 13 IN	Channel 13 High IN
17	Channel 29 IN	Channel 13 Low IN
5	Analog Return	Analog Return
15	Channel 14 IN	Channel 14 High IN
3	Channel 30 IN	Channel 14 Low IN
16	Analog Return	Analog Return
1	Channel 15 IN	Channel 15 High IN
14	Channel 31 IN	Channel 15 Low IN
2	Analog Return	Analog Return

Table 3: DVME-641 External Trigger Input Connections (J3)

PIN #	SIGNAL
1	External Trigger IN*
6	Digital Ground

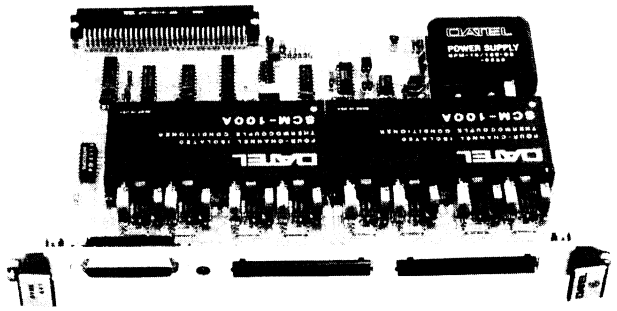
Table 4: DVME-641 Expansion Channel Expansion Connections (J4)

PIN #	SIGNAL
13	Expansion Channel Address Line 0 IN
25	Expansion Channel Address Line 1 IN
12	Expansion Channel Address Line 2 IN
24	Expansion Channel Address Line 3 IN
11	Expansion Channel Address Line 4 IN
23	Expansion Channel Address Line 5 IN
10	Expansion Channel Address Line 6 IN
22	Expansion Channel Address Line 7 IN
4,16	Digital Ground
9	Expansion Channel Address Valid IN
20	Setting Delay OUT*
17	External Trigger OUT*
21	Not Used
5	Not Used
1	Analog Low OUT
14	Analog High OUT
2,15	Analog Common

DVME-643
8-Channel Isolated Analog VMEbus Expansion Board

FEATURES

- **Offers channel expansion to DATEL's DVME-601/611/612 A/D boards**
- **Two models of channel expansion boards**
  DVME-643T: Thermocouple and low-level inputs
  DVME-643H: High-level inputs
- **On-board cold junction compensation sensor**
- **Offers 1000V peak isolation**
- **On-board signal conditioning**
- **120 dB minimum CMRR**
- **55 dB minimum NMR**
- **2.5 millisecond settling time**
- **On-board dc-to-dc power converter**
- **Cascadable to up to 10 MUX boards**
- **Includes a board selection LED lamp**



THE DVME-643 BOARDS OFFER CHANNEL EXPANSION TO DATEL's DVME-601/611/612 A/D BOARDS. THESE MULTIPLEXER BOARDS PROVIDE 1000V ISOLATION AND SIGNAL CONDITIONING FOR EIGHT THERMOCOUPLE, LOW-LEVEL, OR HIGH-LEVEL INPUTS. THE DVME-643T BOARD INCORPORATES A COLD JUNCTION COMPENSATION OUTPUT FOR THERMOCOUPLE INPUTS TO CORRECT AGAINST REFERENCE JUNCTION TEMPERATURE VARIATIONS.

GENERAL DESCRIPTION

Designed specifically for applications requiring multiple channel data acquisition, the DVME-643 boards expand the analog input capability of DATEL's DVME-601/611/612 A/D boards. The DVME-643 boards are offered in two versions. The DVME-643T provides isolation and signal conditioning for thermocouple and low-level inputs. The DVME-643H accepts for high-level voltage and 4-to-20 mA current loop inputs.

The DVME-643T allows mixing thermocouple and low-level signals on the same board. The DVME-601/611/612 boards offer channel expansion for up to 256 channels. In addition to the DVME-643 boards, DATEL's channel expansion boards for high-level and simultaneous sample and hold inputs may also be used with a DVME-601/611/612 board. Figure 1 shows typical multi-channel application configuration.

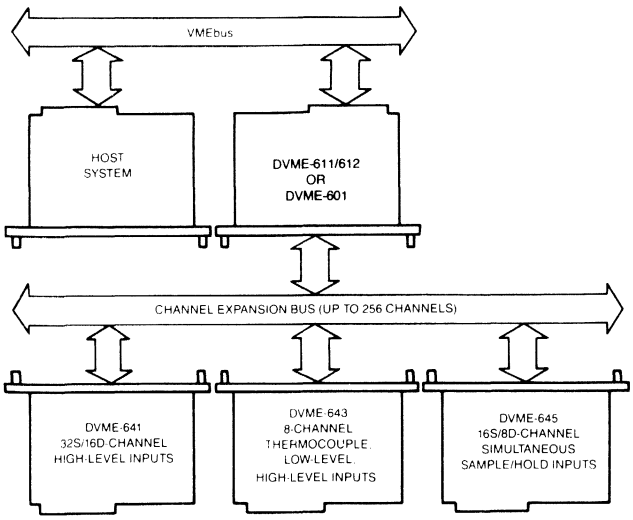


Figure 1: DVME-643 Application Configuration

ORDERING INFORMATION

DVME-643 —

- T — Thermocouple and low-level isolated inputs
  input ranges: ±25.6, 51.2, and 102.4mV
- H — High-level voltage and current loop isolated inputs
  High-level voltage ranges: ±5V dc
  Current loop inputs: 4-to-20 mA

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).
8158760	12-pin connector (included)

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, unless otherwise noted)

ANALOG INPUT

Number of Channels . . . . . 8 Differential and CJC channels

Channel Expansion . . . . . Up to 256S/256D*

Isolation . . . . . 750V RMS
(ch-ch. & ch.-bus) 1000V Peak

Input Range DVME-643T . . . . . ±25.6 mV dc
±51.2 mV dc
±102.4 mV dc
DVME-643H . . . . . ±5V dc

Common Mode Voltage . . . . . 750V RMS
AC, 50 or 60Hz 1000V Peak

Input Bias Current . . . . . 8 nano amperes, maximum

Overvoltage Protection . . . . . 130V RMS, maximum

Input Impedance, ... 100 megohms
differential input to ground

Common Mode Rejection Ratio, f = .01 to 100Hz
DVME-643T . . . . . 120 dB, minimum
DVME-643H . . . . . 110 dB, minimum

Normal Mode Rejection . . . . . 55 dB, minimum
50 or 60 Hz

Settling Time . . . . . 2.5 milliseconds, maximum

dc Gain Accuracy
DVME-643T . . . . . 0.03% FSR, minimum
DVME-643H . . . . . 0.05% FSR, minimum

Gain Drift . . . . . 35 ppm/°C, maximum

Offset Drift
DVME-643T . . . . . 3 μV/°C, maximum
DVME-643H . . . . . 60 μV/°C, maximum

CJC Error
At Room Temperature . . . . . 0.5°C, maximum
At Full Temperature Range . . . 1.5°C, maximum

Output Impedance . . . . . 0.5 K ohms, maximum

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1A typical, 1.5A maximum from P1 VMEbus connector.

I/O CONNECTIONS

The DVME-643 uses J1 and J2 for analog input connections and J4 for channel expansion connections. Tables 1 and 2 list these signals. VMEbus IACK and bus grant signals are daisy-chained.

CONNECTOR SPECIFICATIONS

VMEbus-P1 Connector . . . . . 96-pin male DIN connector

Analog Input J1 and J2 Connectors . . . . . 12-pin male connector

Analog Expansion J4 Connector . . . . . 25-pin D-type female connector, DB-25S

PHYSICAL—ENVIRONMENTAL

Outline Dimensions . . . . . 9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)

Weight . . . . . 1 lb (453.59 grams)

Operating Temperature Range . . 0 to +60°C

Storage Temperature Range . . . . . -20 to +80°C

Relative Humidity . . . . . 0 to 90%, non-condensing

*Up to 10 slave MUX boards may be driven from one A/D master board.

Table 1: Analog Input Connections (J1 and J2)

PIN #	SIGNAL (J1)	PIN #	SIGNAL (J2)
12	Channel 0 High IN	12	Channel 4 High IN
11	Channel 0 Low IN	11	Channel 4 Low IN
10	Analog Return	10	Analog Return
9	Channel 1 High IN	9	Channel 5 High IN
8	Channel 1 Low IN	8	Channel 5 Low IN
7	Analog Return	7	Analog Return
6	Channel 2 High IN	6	Channel 6 High IN
5	Channel 2 Low IN	5	Channel 6 Low IN
4	Analog Return	4	Analog Return
3	Channel 3 High IN	3	Channel 7 High IN
2	Channel 3 Low IN	2	Channel 7 Low IN
1	Analog Return	1	Analog Return

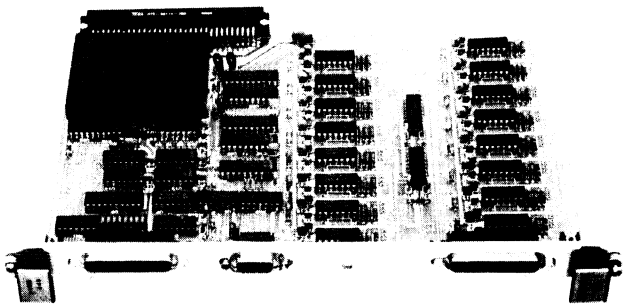
Table 2: Channel Expansion Connections (J4)

PIN #	SIGNAL
13	Expansion Channel Address 0
25	Expansion Channel Address 1
12	Expansion Channel Address 2
24	Expansion Channel Address 3
11	Expansion Channel Address 4
23	Expansion Channel Address 5
10	Expansion Channel Address 6
22	Expansion Channel Address 7
4,16	Digital Ground
20	Settling Delay OUT*
17	External Trigger OUT
9	Expansion Channel Address Valid IN
14	Analog High OUT
1	Analog Low OUT
2,15	Analog Common

DVME-645
16-Channel Simultaneous Sample-and-Hold VMEbus Expansion Board

FEATURES

- **Offers channel expansion to DVME-601/611/612 A/D boards**
- **Offers simultaneous sample-and-hold capability to up to 16S/8D channels**
- **1.2 μV/μS sample-and-hold droop rate**
- **6 Microsecond settling time**
- **Complete compatibility to VMEbus hardware specifications**
- **Cascadable to up to 256 channels**
- **0.05% Full-scale range accuracy**
- **On-board dc-to-dc converter**



THE DVME-645 IS DESIGNED TO PROVIDE CHANNEL EXPANSION TO DATEL'S DVME-601/611/612 BOARDS FOR APPLICATIONS REQUIRING SAMPLE AND HOLD CAPABILITY. THE BOARD IS EQUIPPED WITH 16 SAMPLE-AND-HOLD AMPLIFIERS, ACQUIRING DATA SIMULTANEOUSLY FROM 16 CHANNELS. THE BOARD IS IDEALLY SUITED FOR TRANSIENT ANALYSIS, SIGNAL RECONSTRUCTION AND RELATED APPLICATIONS.

GENERAL DESCRIPTION

The DVME-645 offers simultaneous sample-and-hold capability to DATEL's family of multiplexer boards. The board expands the analog input channels of the DVME-601/611/612 A/D boards. In a typical application, the DVME-645 is usable with other multiplexer boards using thermocouple, isolated and non-isolated voltage inputs. Figure 1 shows the channel expansion to the DVME-601/611/612 A/D boards.

Simultaneous Sample-and-Hold

A sample-and-hold circuit holds or freezes a changing analog input signal for up to a few milliseconds. With 16 on-board amplifiers, the DVME-645 simultaneously holds analog signals from 16 individual channels. An A/D subsystem (DVME-601/611/612) may scan and convert the samples stored. The digital data now represents the analog signal values at an instant of time from all the 16 channels.

The DVME-645 also allows measuring high-speed transients and spikes during a specified window of time. For applications requiring sampling at rates up to 8 MHz all 16 channels may be connected to a single measuring point. The sample-and-hold circuits may then sequentially acquire the analog input signal. In this application, the DVME-645 functions as a very low-cost 8 MHz storage device. Typical applications of the DVME-645 with the DVME-601/611/612 include pulse analysis and reconstruction and data skew elimination for seismic measurements.

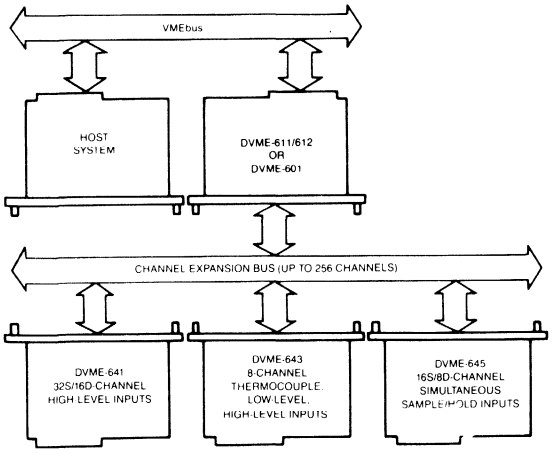


Figure 1: DVME-645 Application Configuration

ORDERING INFORMATION

DVME-645	16S/8D SSH MUX board

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, unless otherwise noted)

Number of Channels . . . . . 16S/8D non-isolated

Channel Expansion . . . . . Up to 256S/256D*

Input Range . . . . . ±10V dc

Analog Output . . . . . Differential

Interface . . . . . Analog expansion bus for DVME-611/612/601 boards

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector . . . . 96-pin male DIN connector

Analog Input J1 Connector 25-pin D-type female connector

External Trigger and Sample-and-hold Control J3 Connector . . . . . 9-pin D-type female connector

Analog Expansion J4 Connector . . . . . 25-pin D-type female connector

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 2.0A typical, 3.0A maximum from P1 VMEbus connector.

I/O CONNECTIONS

The DVME-645 uses J1 and J4 connectors for analog input and channel expansion connections respectively. Tables 1 and 2 list the signals for the connections. Table 3 lists signals for trigger and sample-and-hold control. VMEbus IACK and bus grant signals are daisy-chained.

LED front panel lamp . . . . . lights when board is addressed

ANALOG SPECIFICATIONS

Common Mode Voltage . . . . ±10V dc, maximum

Over Voltage Protection . . . ±35V dc, maximum

Input Bias Current . . . . . 300 nanoamperes, maximum

Input Impedance . . . . . 1 Megohm, minimum

Output Settling Time (For 0 to -10V step input, channel-to-channel settling) . . . . . 6 μseconds, maximum to rated accuracy

dc Gain Accuracy . . . . . 0.05%, minimum

Output Impedance . . . . . 0.5 Kohms, maximum

Input Offset Voltage . . . . . 1.0 mV, maximum

Input Offset Voltage Drift . . . . . 20 μV/°C, maximum

Aperture Delay . . . . . 50 nS

Aperture Time . . . . . 100 nS

Sample-and-Hold Droop Rate . . . 1.2 μV/μS, typical
2.0 μV/μS, maximum

Sample-and-Hold Pedestal . 1.0 mV, typical
2.5 mV, maximum

PHYSICAL—ENVIRONMENTAL

Outline Dimensions . . . . . 9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)

Weight . . . . . 12.5 Oz. (354.75 grams)

Operating Temperature Range . . . . 0 to +60°C

Storage Temperature Range . . . . . 20 to +80°C

Relative Humidity . . . . . 0 to 90% non-condensing

Table 1: DVME-645 Analog Input Connector (J1)

PIN #	Single-ended	Differential
24	Channel 0 IN	Channel 0 High IN
12	Channel 8 IN	Channel 0 Low IN
25	Analog Return	Analog Return
10	Channel 1 IN	Channel 1 High IN
23	Channel 9 IN	Channel 1 Low IN
11	Analog Return	Analog Return
21	Channel 2 IN	Channel 2 High IN
9	Channel 10 IN	Channel 2 Low IN
22	Analog Return	Analog Return
7	Channel 3 IN	Channel 3 High IN
20	Channel 11 IN	Channel 3 Low IN
8	Analog Return	Analog Return
18	Channel 4 IN	Channel 4 High IN
6	Channel 12 IN	Channel 4 Low IN
19	Analog Return	Analog Return
4	Channel 5 IN	Channel 5 High IN
17	Channel 13 IN	Channel 5 Low IN
5	Analog Return	Analog Return
15	Channel 6 IN	Channel 6 High IN
3	Channel 14 IN	Channel 6 Low IN
16	Analog Return	Analog Return
1	Channel 7 IN	Channel 7 High IN
14	Channel 15 IN	Channel 7 Low IN
2	Analog Return	Analog Return

Table 2: DVME-645 Expansion Connections (J4)

PIN #	SIGNAL
13	Expansion Channel Address Line 0 IN
25	Expansion Channel Address Line 1 IN
12	Expansion Channel Address Line 2 IN
24	Expansion Channel Address Line 3 IN
11	Expansion Channel Address Line 4 IN
23	Expansion Channel Address Line 5 IN
10	Expansion Channel Address Line 6 IN
22	Expansion Channel Address Line 7 IN
4,16	Digital Ground
9	Channel Address Valid IN
8	Start Conversion Strobe IN
20	Strobe Delay OUT*
7	End of Conversion IN
19	End of Scan IN
17	External Trigger OUT*
6	General Purpose Input (XMODSEL)
5,21	Not Used
1	Analog Low OUT
14	Analog High OUT
2,15	Analog Common

Table 3: DVME-645 Digital Control Connections (J3)

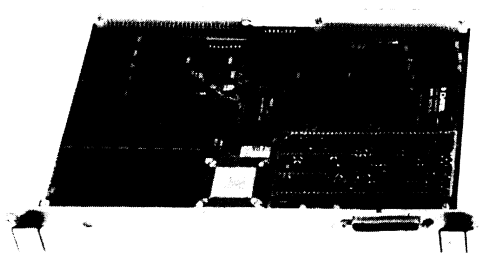
PIN #	SIGNAL
1	External Trigger IN*
6	Digital Ground
9	Sample/Hold Skew IN
5	Sample/Hold Skew OUT
3	Sample and Hold Skew Clock IN/OUT
4	Sample and Hold Control IN/OUT

*Up to 10 slave MUX boards may be driven from one A/D master board at derated settling.

DVME-630
Very High Speed A/D-DSP Coprocessor Board for VMEbus Computers

FEATURES

- **Up to 4 MHz A/D sample rate**
- **Up to 16S/8D analog input channels**
- **Choice of 12 or 14-bit A/D resolution**
- **4-channel Simultaneous Sample/Hold's are optional**
- **On-board 320C30 32 MHz Digital Signal Processor**
- **512 Kilobyte Dual-Ported RAM**
- **Two 1K x 32 internal DSP RAM**
- **8K x 32 Expansion RAM**
- **On-board DSP Library - FFT's, filters, matrix math, floating point, etc.**
- **Fast, simple, powerful command Executive**
- **No local programming required.**
- **Vectored Interrupt to VMEbus host**



DESCRIPTION

Advanced performance from the DVME-630's on-board Digital Signal Processor (DSP) offers a broad range of high speed waveform analysis and recording applications. The DVME-630 will acquire up to sixteen analog input channels, digitize them and store them in local memory while DSP math processing and data transfer is done concurrently. The system is intended for preprocessing "seamless" A/D data streams to the host system.

The DVME-630 is ideal for non-stop, continuous Fast Fourier Transform (FFT) processing, communications receiver signal collection to disk or simultaneous graphics display of spectral data. Application areas include signal recovery from noisy channels, harmonic distortion analyzers and vibration/resonance filtering systems. For use with ultrasonic, sonar or acoustic signals, the interrupt-driven, simultaneous block transfers of data insure no information loss. Other uses include high speed mapping and imaging, satellite channels, astrophysics, seismology, biomedical signals, array processing, control systems, simulators, engine analyzers, aerodynamics and vehicle systems.

The board consists of a pluggable analog input subsection, timer-counters, DSP central processing unit (CPU), dual port RAM, local RAM, bus interface, registers and DC power supply. Input signals pass through a very high speed channel multiplexer (except model DVME-630D) to a sampling analog-to-digital (A/D) converter. On model DVME-630A, all four channels are acquired simultaneously by a quad simultaneous sample/hold (SSH) section. A choice of channels, input ranges, speeds and resolution is offered in the analog section.

A/D triggering for spectral and FFT applications must be precisely controlled. This is handled by a programmable timer-counter section which can control the interval between A/D conversions and the interval between multi-sample A/D

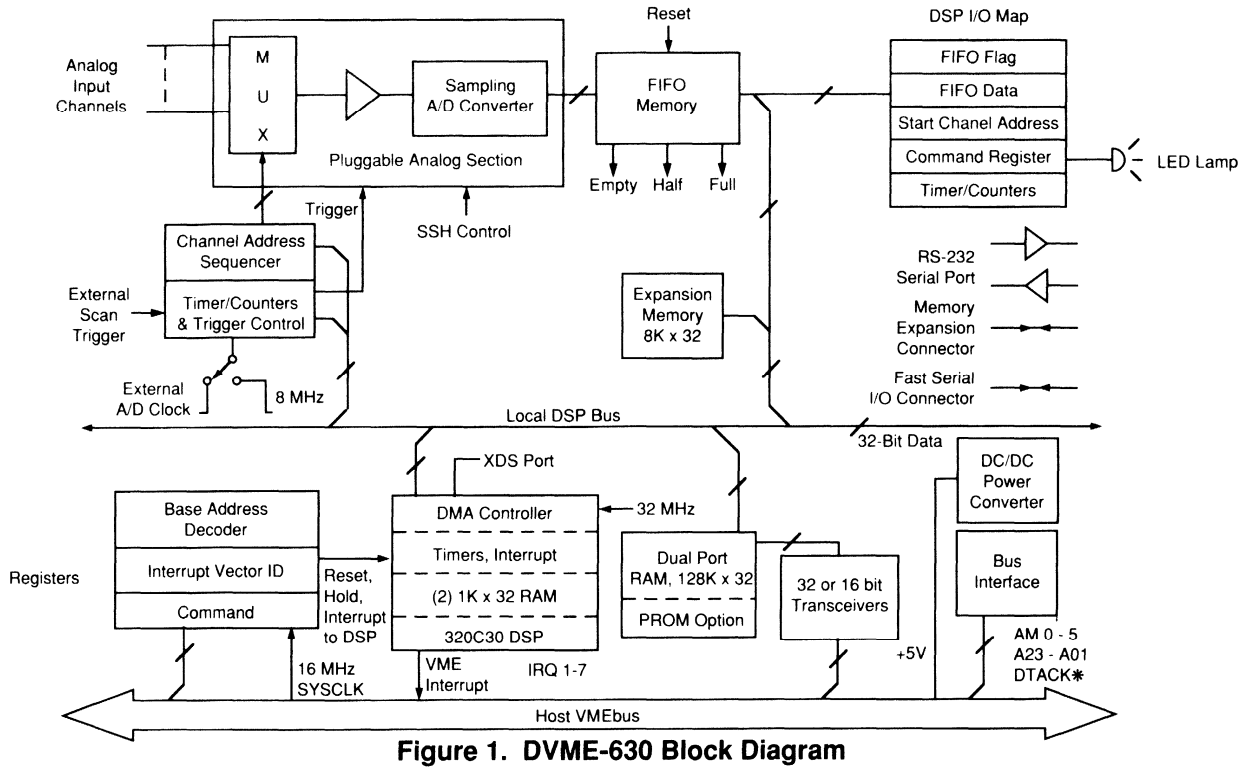


Figure 1. DVME-630 Block Diagram

scans. The number of samples may also be counted for repeating array sampling. The timer-counter may use an on-board crystal oscillator or an external timebase for precision phase-tracking.

The digital output of the A/D passes directly to a first-in, first-out (FIFO) memory. The FIFO acts to decouple the precision timing of the A/D section with the block transfers governed by the DSP internal direct memory access (DMA) controller. Additional timers internal to the DSP are also used.

A/D FIFO data may be sent to dual port random access memory (DPR) shared with the host VMEbus. The DPR is organized as 128K by 32 bits of fast static RAM. The user may also set up the DPR as 256K by 16 bits, allowing all access using only the P1 port if needed. Local A/D-FIFO block transfers are controlled by the DMA controller in the DSP. The DMA may run in background while math processing continues. Local FIFO and DMA TC interrupts to the DSP arbitrate these activities. Typically, a swapped dual buffer method is used so that samples are not lost during other processing. Local hardware registers control all A/D, FIFO and trigger activity.

Single cycle fetch and execution, zero-overhead of looping instructions, software variable wait-states, block repeat and an internal instruction cache memory are some of the advanced high speed features of the Texas Instruments 320C30 DSP. The DSP uses 32-bit local data paths for very high speed. Simultaneous access attempts to the DPR by both the VMEbus host and the DSP are resolved by high speed arbitration logic. The DSP also has a separate 8K by 32-bit local expansion memory for the stack or temporary data. The architecture of the DSP allows simultaneous processing of two tables from two sections of memory. This provides optimum processing of FFT's and other array functions.

The DVME-630 DPR appears as both read/write memory addresses and as two hardware control registers mapped into the top of the DPR. The registers include a command register and a software programmable interrupt vector ID register. The DVME-630 will operate with all 680X0, 880X0, 80X86, RISC and SPARC CPU's. The DPR base address may be located anywhere up to 16 megabytes on 256 kilobyte boundaries. The board will also operate with all popular operating systems including SUN, UNIX, OS-9, PDOS, pSOS, MS-DOS, VRTX and others.

Executive Software

Access to the on-board DSP library and all A/D-timer functions is provided in the Executive software package. After loading in the Executive from host disk to the DPR, the DSP is transitioned from reset to run using a command register control bit. The board may be reset at any time using this technique. The comprehensive Executive software package offers fast A/D sample collection and DSP math without writing any local programs. A simple, powerful, high speed command list is used to access the local DSP library. On the VMEbus side, the Exec driver controls very fast buffer transfers to disk or memory using VMEbus bus interrupts generated from the DVME-630. Either host DMA transfers or CPU program transfers may be used. Host interrupt levels are also jumper programmable. Software is available in professionally-written, heavily-commented "C" source format on popular disk media. The software is highly portable to most VME platforms.

FUNCTIONAL SPECIFICATIONS

(Typical at +25 °C, dynamic conditions, Gain = 1, unless noted)

ANALOG INPUTS			
Number of Channels	4 channels (models A,B,C) 1 channel (model DVME-630D) 16S/8D channels (DVME-630E)		
Input Configuration	single-ended, non-isolated		
Full Scale Input Ranges (user-selectable)	0 to +10V ±10V	±5V	±1V
DVME-630A	yes	no	2 chans. gain = 10
DVME-630B	yes	yes	no
DVME-630C	yes	yes	no
DVME-630D	no	no	±1.25V
DVME-630E	yes	yes	note 8
Programmable gain	models A and E, see note 8		
Input Impedance [Note 5]	10 MΩ, min. power on (160 KΩ,630D) 1.5 Kilohms power off		
Input Bias Current	±1 nA		
Input Capacitance	10 pF per channel		
Input Overvoltage	±15V (no damage)		
Overvoltage Recovery Time	2 microseconds max.		
Common Mode Voltage Range	±10V max. referred to analog common (630E)		
Common Mode Reject.	-80 dB (g = 100) 630E only [DC to 60 Hz]		
Addressing Modes	1. Single channel 2. Simultaneous Sample/Hold (DVME-630A only) 3. Sequential with autosequenced addressing 4. Random addressing by host software		
SAMPLE/HOLD			
Acq. Time (FSR step) to 0.01% of FSR	750 nS max. (DVME-630A,B,E) 200 nS max. (DVME-630C) 50 nS max. (DVME-630D)		
Aperture Delay	6 nS (DVME-630A) 30 nS (DVME-630B,C,E) 10 nS (DVME-630D)		
Aperture Delay Uncertainty	±1 nS (DVME-630A) ±5 nS (DVME-630B,C,E) ±10 pS (DVME-630D)		
Droop Rate	1 µV/µS		
SSH Chanel-to-Channel Linearity Tracking (DVME-630A only)	± 0.03%		
A/D CONVERTER			
Resolution	12 bits (DVME-630A,C,D,E) 14 bits (DVME-630B)		
Conversion Period	500 nanoseconds (DVME-630A) 1 microsecond (DVME-630B,C,E) 200 nanoseconds (DVME-630D)		
Output Coding	Positive-true right-justified straight binary (unipolar) or right-justified two's complement (bipolar) with sign extension through bit 15.		
A/D Trigger Sources (Software selectable)	1. Local Pacer sample clock 2. External TTL sample clock		

TOTAL SYSTEM DC CHARACTERISTICS G = 1 [Note 6]	
Integral Non-linearity at +25 °C	±1 LSB of FSR (630A,C,E) ±1.5 LSB of FSR (630B,D)
Diff. Non-linearity at +25 °C	± 0.75 LSB of FSR (630A,C,E) ± 1 LSB of FSR (630B,D)
Full Scale Temperature Coefficient	±0.1 LSB per °C (630A,C,E) ±0.3 LSB per °C max (630B,D)
Zero or Offset Temp. Coefficient	±0.1 LSB per °C max (630A,C,E) ±0.3 LSB per °C max (630B,D)
Power Supply Reject.	±0.004% per % of bus +5V

A/D MEMORY	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024 A/D samples, standard. 4096 samples optional.

TOTAL SYSTEM DYNAMIC PERFORMANCE [Note 1]	
System Bandwidth (single channel, half-scale input)	1 MHz (630A,C) 200 KHz (630B,E) 2.5 MHz (630D)
Total Throughput to FIFO (single channel, gain=1)	700 nanoseconds (630A) 2 microseconds (630B,E) 1 microsecond (630C) 250 nS (630D)
Throughput to FIFO per A/D sample (sequential channels, gain = 1) [Note 3]	1 microsecond (630A) 3 microseconds (630B) 2 microseconds (630C) 4 microseconds (630E)
Throughput to FIFO (sequential channels, gain = 10)	10 microseconds (630A)
Total Harmonic Distortion (Note 2)	-72 dB (630A,C,E) -75 dB (630B) -68 dB (630D)

TRIGGER CONTROL	
Programmable Timer/Counter Type	82C54
Functions	1. A/D sample count reached. 2. A/D start rate (16 bit divisor) 3. Scan trigger rate (16 bit divisor)
Pacer Sample Counter	1 to 65,536 samples. Drives the Acquire flag gate for A/D start pulses. Larger sample blocks may be programmed.
Timer Clock Source (User-selectable)	1. Internal 8 MHz crystal clock 2. External TTL input, 10 MHz max.

LOCAL MICROCOMPUTER	
CPU Type	Texas Instruments TMS 320C30 Digital Signal Processor
Local Data Bus	32 bits
CPU Clock Speed	32.000 MHz
Local DMA Controller	Internal to 320C30 CPU
Primary Memory (Dual ported to VMEbus)	128K x 32 static RAM
PROM Option	32K x 32 of primary memory may be replaced by user-programmed Read Only Memory. Additional wait states may be needed during PROM access.
Expansion Memory (No VMEbus access)	8K x 32 static RAM
Internal DSP Memory	Two 1K x 32
Dual Port Access from VMEbus	Hold mode by control bit or dynamic hold per each access.
CPU Test Port	Supports TI XDS1000 Extended Development System.
Local Interrupts to DSP	Int 0-3 from VME host request, A/D FIFO or sample count acquire flags or optional external interrupt.
Wait States	May be software programmed via CPU register up to 7 waits. Defaults to 7 waits at reset.

VMEbus INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Data Bus Width	16 bits using P1 connector or 32 bits using P1 and P2. Changed by alternate transceiver sockets on board.
Address Bus	24 address lines (A23-A1) plus 6 Address Modifiers.
Address Modifier Codes	39 hex or 3D hex, selectable.
VMEbus Interrupt	1 line, selectable IRQ 1-7*. Asserts maskable programmable 8-bit vector ID code.
VMEbus Interrupt Source	via DSP I/O bit (software programmable).
Architecture	SAD24:SD16 or SAD24:SD32 memory-mapped slave consisting of 128K x 32-bit longwords of dual ported RAM. The DVME-630 is not a bus master. A small register area overlays the top of the DPR. DSP location 0 is mapped at the bottom of DPR.
Control/Status Functions	DSP halt request, DSP reset/run, VME interrupt enable/disable, vector ID R/W, force local maskable interrupt to DSP.
Data Transfer	Uses 16 MHz VMEbus SYSCLK signal (required) to generate DTACK* with selectable delay in 125 nS steps. Will accept host DMA controller access.

CONNECTORS	
VMEbus, P1 and P2	Two 96-pin male DIN connectors.
Analog Input Connect	Four miniature threaded SMA coaxial (for high frequency inputs), or DB-25S (for medium frequency inputs).
Trigger Connector	5th coax connector or DB-25 for external trigger input.
Memory Expansion (32-bit data)	72-pin header, unbuffered. Uses 0.025" square pins, 0.100" spacing.
XDS CPU Port	12-pin header, 0.1" pinning.
Fast CPU Serial I/O [Incl. trigger, clock, etc.]	20-pin header, unbuffered, 0.1" pinning.
RS-232-C Asynch. Serial Port [uses software UART]	3-pin header (Xmt, Rcv, Gnd), 0.1" pinning.
MISCELLANEOUS	
LED Lamp	Front panel green LED lamp may be controlled by internal register bit for alarms, etc.
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain per channel for SSH on DVME-630A. A single offset and gain pot is provided on DVME-630B,C,D,E. Recommended recalibration interval is 90 days in stable conditions.
Power Required	+5V dc ±5% at 4 Amps max. from VMEbus.
Operating Temp Range	0 to +60 °C. Forced cooling is recommended.
Storage Temp Range	-20 to +85 °C
Relative Humidity	10% to 90%, non-condensing.
Altitude	0 to 10,000 feet.
Outline Dimensions	Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233,5 x 160 x 15,24 mm).
Weight	22 ounces

NOTES

1. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

2. THD test conditions are:
   a. Input frequency — 500 KHz (DVME-630A)
      200 KHz (DVME-630B,E)
      300 KHz (DVME-630C)
      1 MHz (DVME-630D)
   b. Generator/filter THD is -90 dB min.
   c. THD computed by FFT to 5th harmonic.

$$THD = 20 * \log 10 \quad \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{V_{IN}}$$

   d. Inputs are 1/2 full scale. No channel advance.
   e. A/D trigger rate=1.5 MHz (DVME-630A), 500 KHz (DVME-630B,C,E), 4 MHz (DVME-630D)

3. The rates shown for sequential sampling are the maximum A/D converter start rates and include required MUX sequencing and settling delays. For example, if four channels of the DVME-630C were scanned, the maximum sample rate on any one channel would be 2 microseconds X 4 channels = 8 microseconds (125 KHz per channel).

4. To avoid overload recovery delays, do not let the analog input exceed ±10 Volts.

5. The input impedance of 10 Megohms minimum avoids attenuation errors from external input source resistance. For many applications, an inline coaxial 50-ohm shunt, inserted adjacent to the front connectors, is recommended to reduce line reflections and standing wave errors.

6. Allow 20 minutes warmup time to rated specifications for model DVME-630B.

7. The DVME-630 must be mapped in the physical memory of the host VME computer. On some operating systems (notably UNIX), a physical-to-logical addressing function supplied with the OS is used to access the board. The OS may need to know about this absolute physical memory reservation at boot-up time using a device driver. See the example programs available with the DVME-630.

8. Programmable Gain

Gains from x1 to x100 are available on the DVME-630E by installing a precision resistor. Additional settling delay will be needed at higher gains. Fixed gains of x1 and x10 on two channels are selectable on the DVME-630A. They offer 1 Volt input ranges.

Simultaneous Sample/Hold

As shown in Figure 2, four input signals are sampled at the same time using the DVME-630A's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors from conventional multiplexer scanning.

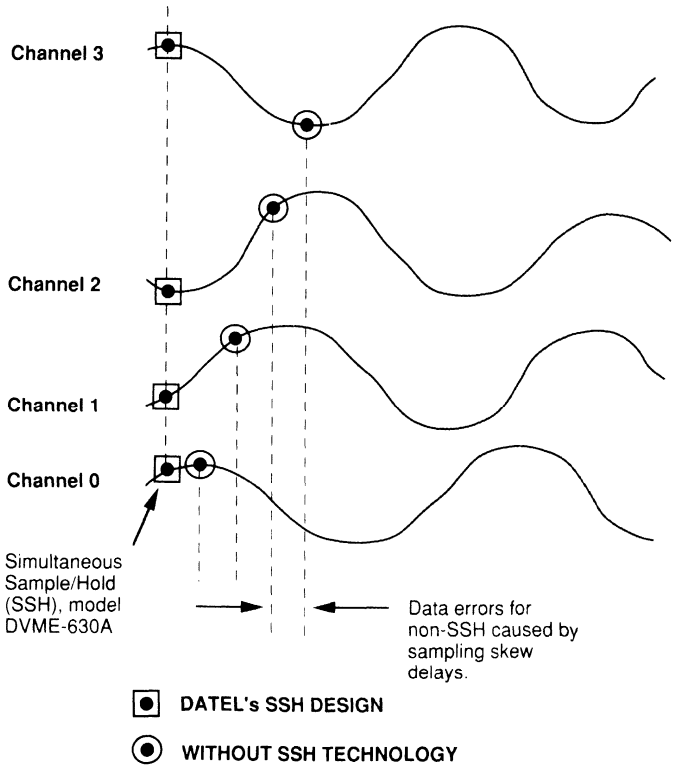


Figure 2. DVME-630A Simultaneous Sample/Hold

DVME-630 Software

The DVME-630 system has been designed to optimize three competing objectives:

Easy to Use (no local programming)
Fast
Powerful (access to full DSP library)

To achieve these mutually exclusive goals, a high speed command list form of control is used. The Application Function Block (AFB) is a short list calling local library functions. No local programming is needed. The user writes the AFB file with any text editor and it is then converted on the VMEbus side to an internal binary form. The converted AFB is then downloaded to DVME-630 Dual Port RAM (DPR) and executed. The AFB is powerful because of full access to the local DSP library and because repeating functions may be looped. These loops in turn may be nested. Loops can run with a loop count or "forever" until stopped.

Unlike a slow ASCII interpreter, the AFB runs at the full speed of the 320C30 DSP with minimal overhead. And to accept fast A/D's without sample loss, only a fully integrated hardware/software system will handle the bandwidth. This hardware system consists of local FIFO A/D memory, local FIFO interrupts and a local Direct Memory Access (DMA) controller inside the DSP which runs in background. FIFO interrupts cause DMA data block transfers while the DSP continues foreground processing.

Executive Package

The complete Executive software package is an integrated environment for full control of the DVME-630. It includes programs which run on both the host VMEbus and the DVME-630. The Executive package consists of:

The AFB ASCII to binary file converter (AFBCNVRT).
A small menu shell.
The VMEbus Host Driver package.
The Executive scheduler, DSP library, boot code, vectors and full local DVME-630 system.

To use this environment, the user simply converts the AFB text file to a binary file, downloads this to the DVME-630 through the Driver and retrieves data files.

DVME-630 Host System Architecture

(See Figure 4)

When the DVME-630 is fully installed, the host VME memory map contains the resident library, the Interrupt Service Routine, a small menu program and the DVME-630's dual port RAM. These systems all work together to provide fast disk or buffer transfers of DSP'd A/D data. The entire system is controlled by simple user-written command files.

Software Hierarchy

The relationship between software in the VMEbus host and in the DVME-630 is illustrated in this diagram. Control flows downward from the user's AFB and A/D data flows upward.

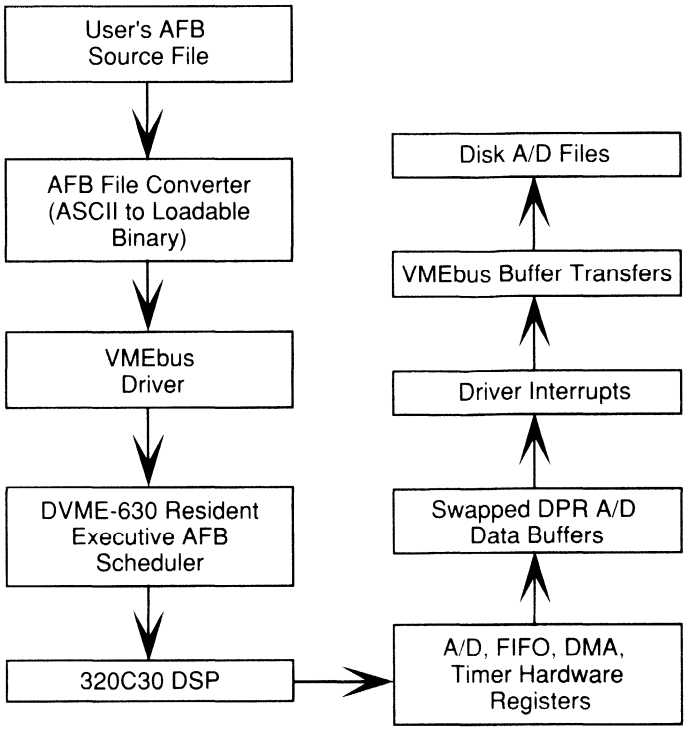


Figure 3. Software Hierarchy Flow Chart

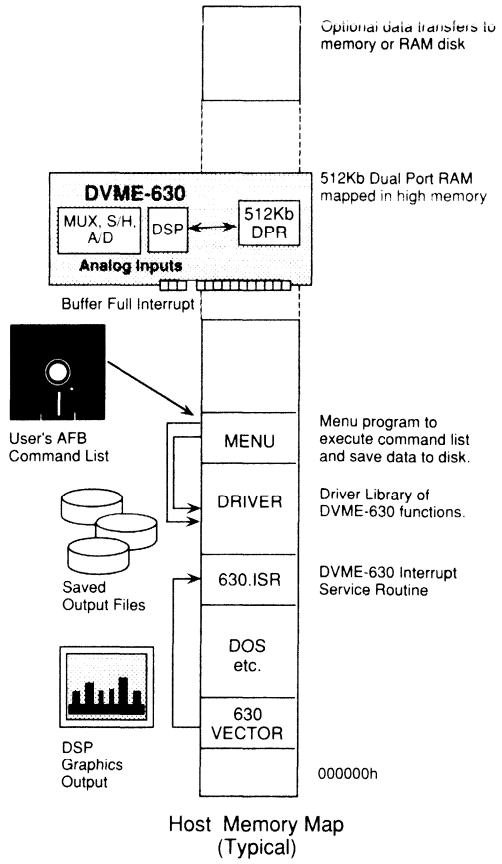


Figure 4. DVME-630 Host System Architecture

Library Functions

The following functions are downloaded at power up by the Driver to the DVME-630 DPR and form the resident on-board DSP library. They may be called from the DPR by including them in the user's downloaded AFB.

A/D Scan Routines

initad	Initialize the start channel address.
inittim1, inittim2, inittim3	Initialize timers 1, 2, or 3.
sadtsc	Select internal or external A/D trigger source.
sadcr	Select the A/D internal conversion rate.
sstr	Select the internal scan trigger rate.
sadspc	Select the number of A/D samples.
stads	Set the total number of A/D samples under 65K. (For 65K or greater, refer to the special techniques).
sfifoi	Enable or disable local FIFO interrupts.
sadr	Enable or disable A/D conversions.
rfifo	Reset FIFO.
calad	Calibrate A/D single samples.
dma_intrpt	Enable or disable FIFO DMA interrupts.
fifoisr	FIFO local Interrupt Service Routine.
scommreg	Set A/D command register.

DSP Array Routines

fir	Do FIR filter on array with user-supplied coefficients.
iir	Do IIR filter on array with user-supplied coefficients.
linfir	Convolution on linear array.
cirfir	Convolution on circular array.
windham, windhan	Multiply a Hamming or Hanning window with signal data array.
windrec	Multiply a rectangular window with signal data array.
windblh	Multiply a Blackman-Harris window with signal data array.
windrco	Multiply a Raised Cosine window with signal data array.
cfftc	Do complex Fast Fourier Transform (FFT) on array.
fft	Do real FFT on array.
twiddle_c	Generate complex array of bit-reversed twiddle factors.
twiddle_r	Generate array of twiddles for real FFT.
dct	Do Discrete Cosine Transform on array (for signal compression).
magfft	Calculate magnitude of real FFT array.
dbfft	Performs log10 on FFT array to prepare data for graphic display.
call_sine, call_cos	Generate sine or cosine arrays.
call_const	Fill array with constant.
bitrev	Shuffle array with bit reverse addressing.

Array Conversion Routines

(The 320C30 DSP uses an internal 32-bit floating point format which is optimized for hardware speed)

ieeedsp	Convert IEEE-754 floating point array to 320 format.
dspieee	Convert 320 array to IEEE-754 floating point format.
matadd	Doubleword matrix addition on array.
matmul	Doubleword matrix multiplication on array.
hstgrm	Histogram of doubleword array.
int2float	Convert doubleword integer array to 320 floating point.
float2int	Convert 320 floating point array to doubleword integers.
sign_extend	Convert an array of 12, 14 or 16-bit A/D data to 32-bit signed integer format.
float_transfer	Sign extend A/D data, convert to floating point and block transfer between buffers.

Single Variable Transcendentals

sine, cosine, tangent
hyperbolic sine, cosine, tangent
inverse sine, cosine, tangent
square root, powers, exponential
natural logarithm, Base10 logarithm

(These functions are available in the TI "C" compiler library)

Buffer Management

defsbuf, defdbuf	Define single and double buffers.
set_ibuf, set_obuf	Setup input and output double buffers. Post current buffer addresses in Exec status area. Interrupt the VME host that data is ready. Flag overflow errors. Used for non-stop A/D filling without sample loss.
ibuf_ready, ibuf_release	Used to sequence each swapped buffer FIFO DMA transfer.
switch_buffers	Swaps buffer pointers under AFB control.
unrav2, unrav4	Separate one array of sequential multi-channel data into two or four single channel arrays.
concat	Compress an array of one A/D sample per 32-bit longword into an array of contiguous 16-bit A/D words. Concat forms a single 32-bit longword from the 16-bit LSB's of two longwords. MSB's are discarded.
dprxfer	Do swapped double buffer block transfers within DVME-630 local memory using buffer numbers.
addxfer	Do block transfers within DVME-630 local memory between absolute addresses. Overlapped transfers will preserve data.
int2pc	Select buffer ready or local timer interrupt to VMEbus.

VME Host Driver

The final portion of the full Executive package is the Driver containing a library of functions to control the DVME-630. This offers a simple menu to control the DVME-630. No programming is required. Because of the modular design of the driver, its functions may be used through the menu shell or may be controlled by a user's program after rewriting the menu shell.

The Driver functions are:

- Install VMEbus Interrupt Service Routine (ISR) to respond to DVME-630 buffer full flags.
- Initialize the VMEbus interrupt system.
- Set the DVME-630 memory base address and test memory.
- Download the Exec, library and full local system to the DVME-630 DPR from a system binary file.
- Boot the local DVME-630 system and confirm.
- Allocate a VMEbus Host buffer to receive DVME-630 data.
- Download a converted AFB file and start execution.
- Collect data to buffer or disk using swapped double buffer interrupts.
- Stop the AFB and save the DVME-630 data buffer to a file.
- Load and run a user COFF object file.
- Calibrate the A/D. Halt and reset the DSP. Quit to the OS.

VMEbus Memory Map

	Byte Address
Interrupt Vector ID (Read/Write)	Base+7FFFFh
Command Register (Write Only)	Base+7FFFCh
Not Used	Base+7FFF8-Bh
Dual Port Random Access Memory	Base+7FFF7h (512 Kb)
	Base (DSP location 0)

Command Register (Write Base+7FFFCh)

Bits 0 - 3: Not used
Bit 4: VME interrupt enable
Bit 5: DSP interrupt request
Bit 6: DSP hold request
Bit 7: DSP reset/run

AFB Source File Format

The AFB source format uses symbolic names for internal DVME-630 library functions. The ASCII file may be written in free form with the user's choice of loop nesting indentation, skipped lines, etc. Comments after the function name delimiter are ignored. After the user writes the AFB, the AFBCNVRT file converter prepares a binary output file which is subsequently downloaded through the Driver for execution. Here is an AFB example which defines buffers, generates a sine wave, then prepares an FFT array for floating point output:

```
DEFDBUF,          ;function to define double buffer
0x0L,             ;starting buffer number
0x400L,           ;buffer length
0x200L,           ;alignment

DEFSBUF,          ;define single buffer for twiddles
0x2L,             ;buffer number
0x100L,           ;buffer length
0x100L,           ;alignment

TWIDDLE_R,        ;generate twiddle factors
0x2L,             ;buffer number 2

BEGIN,            ;begin flag
FOREVER,          ; -1 = loop forever flag

CALL_SINE,        ;fill buffer with sine array
0x00000000L,      ;buffer number 0
0x00000020L,      ;period of the sine wave

FFT,              ;do FFT on buffer
0x0L,             ;buffer number 0
0x200L,           ;number of points
0x9L,             ;Log 2 of number of points
0x2L,             ;buffer for twiddle factors

MAGFFT,           ;take magnitude of FFT data
0x0L,             ;buffer number 0
0x200L,           ;FFT size

DSPIEEE,          ;convert to IEEE format
0x0L,             ;buffer number 0
0x100L,           ;buffer length

SET_OBUF,         ;interrupt to VMEbus that buffer is
                  ready
0x0L,             ;buffer 0
0x100L,           ;buffer length
SWITCH_BUFFERS    ;swap double buffers

END               ;end flag for this loop
```

ORDERING GUIDE

Model	A/D Bits	FIFO Size (Samples)	Chans.	Sample rate single chan.	Simul.S/H	PGA
DVME-630A1	12	1024	4s	1.5 MHz	4 chans.	x1,x10 (two chans.)
DVME-630A2		4096				
DVME-630B1	14	1024	4s	500 KHz	none	none
DVME-630B2		4096				
DVME-630C1	12	1024	4s	1 MHz	none	none
DVME-630C2		4096				
DVME-630D1	12	1024	1s	4 MHz	none	none
DVME-630D2		4096				
DVME-630E1	12	1024	16s/8d	500 KHz	none	X1 to X100
DVME-630E2		4096		(1 chan.)		resistor select

DVME-630EXEC

Executive software package in "C" source format on IBM-PC/AT high density 5.25" and 3.5" disks. Includes all local functions in downloadable binary format.

DVME-630SRC

Source code for all DSP local functions, boot code, vectors, scheduler, DSP math library, A/D, FIFO/DMA, buffer management and timer/counter function library. Supplied in "C" and Texas Instruments 320C30 Assembly language. IBM-PC/AT HD 3.5" and 5.25" disks.

(Contact DATEL for other media)

Each board is power-cycle burned-in, tested and calibrated. All models include a user's manual. The warranty period is one year.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

DVME-622
8- or 16-Channel Fast Simultaneous Analog Output Board for VMEbus Computers

FEATURES

- **8 or 16 analog outputs**
- **12-bit D/A resolution**
- **3 microsecond settling time**
- **Simultaneous update**
- **Trigger timer interrupt**
- **Digital I/O (4-in, 3-out)**
- **Output ranges selectable per channel**

DESCRIPTION

Many applications require phase-synchronous analog outputs. Examples include precision system simulation and coherent field generation in process control, audio, acoustics and sonar. The DVME-622 is a high density analog output board with up to 16 signal channels. Each Digital to Analog Converter (DAC) channel may be individually selected for full scale output ranges of 0 to +5V, 0 to +10V, ±5V or ±10V. All outputs are buffered and will deliver ±0.025% accuracy from 0 to 5 milliamps output load. The DVME-622 is installed in a host VMEbus computer.

To achieve the simultaneous update capability, each channel input register is double buffered. The registers are successively loaded by the host computer then all channels are updated by host command or trigger. If preferred, each channel may also be operated in the non-concurrent transparent mode under program control with random addressing or single channel operation.

For applications requiring a precision clock to sequence the output waveforms, the DVME-622 includes a software-programmable trigger. The trigger strobes the simultaneous update and posts a status bit or interrupt to the host computer. Upon detecting the trigger, the host may block-load the next data frame. The trigger may be derived from an internal crystal-stabilized timer or from an external timebase. The external trigger option makes the DVME-622 fully synchronous with external events. The trigger section also includes a spare output counter, usable for any purpose.

For repeating frame scan applications, the DVME-622 includes an autoincrement mode. In this mode, block transfer instructions will automatically load up to 16 channels at very high speed from a memory buffer in the host. The DVME-622 will digitally steer each analog data word to successive DAC input registers while using the same memory data register address. The user's program simply maintains a CPU register as a downcounter to terminate each block transfer. Typically, the trigger and autoincrement modes are used together where the host loads the next block after detecting the trigger status signal from the last simultaneous update.

The combination of a precision frame clock trigger, autoincrement channel addressing and high speed simultaneous block loading make the DVME-622 ideal for artificial waveform applications. Such waveform generators continuously loop through a large RAM buffer containing a synthetic composite digitized analog signal.

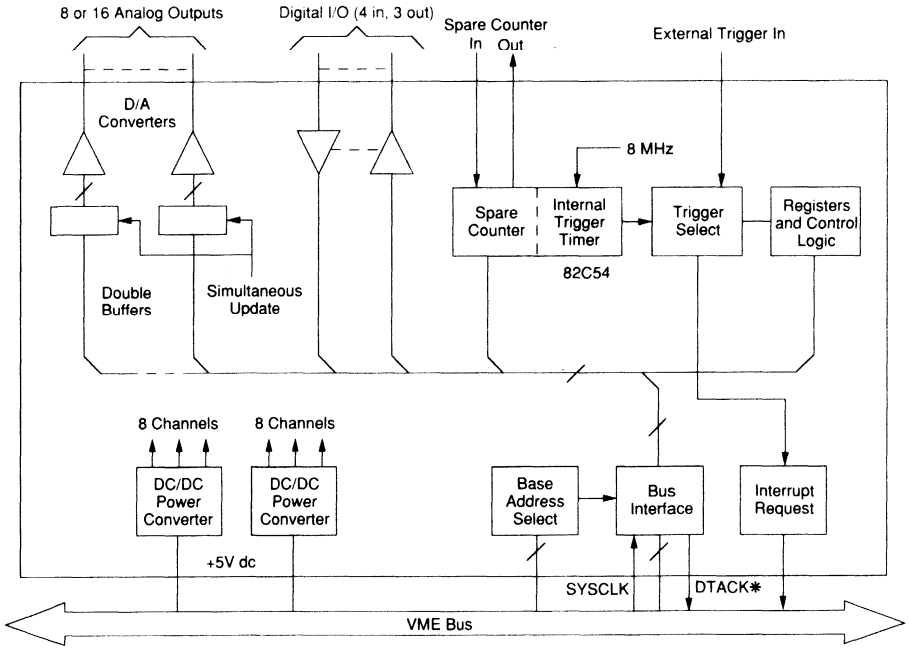


Figure 1. DVME-622 Block Diagram

ORDERING GUIDE

Model	Number of channels
DVME-622A	8
DVME-622B	16

The board is fully tested and includes a user manual plus setup and configuration source program on MS-DOS disk. The program provides calibration and test waveforms.

Fast settling rates are another feature of the DVME-622. Full scale step response of each DAC channel is 3 microseconds. Block transfers of input data may occur faster than individual DAC channel analog settling times. Each DAC channel input register can be updated at over 1 Megasample per second.

The DVME-622 is configured on a 6U VME compatible board. Analog signal connections are made using a front panel 25-pin "D" connector. Seven digital channels (4 inputs and 3 outputs) of discrete I/O are provided for general purpose control and monitoring of external logic devices. A 9-pin "D" connector provides digital I/O. The DVME-622 includes two high efficiency DC to DC power converters to supply local analog circuits. The entire board uses only +5 Volt DC power from the VME bus. The board is compatible with all popular computer languages although the highest speed will require assembly language. A comprehensive user's manual is included with the board showing full programming and application information.

SPECIFICATIONS

(typical at +25 °C, dynamic conditions, unless noted)

ANALOG OUTPUTS	
Number of Channels	8 or 16
Output Configuration	single-ended, non-isolated
Full Scale Output Ranges	0 to +5V, 0 to +10V, ±5V, ±10V, individually selectable per channel.
Output Current	0 to ±5 mA min. (source or sink), short-circuit protected to ground.
Resolution	12 binary bits.
Input Data Coding	Straight or offset binary, positive true coding. Data is right justified. See note 3.
Output Impedance	50 milliohms
Channel Addressing Modes	Random, simultaneous or auto-increment sequential.
PERFORMANCE	
Monotonicity	No missing codes
Linearity Error (after calibration)	±0.025% of FSR.
Temperature Coefficient of Gain	±5 ppm typ., ±30 ppm max. of FSR/ °C max.
Temperature Coefficient of Zero or Offset	±20 ppm of FSR/ °C max.
Settling Time (FS step)	3 microseconds max. to ±0.025% of final value. (0-5V, 0-10V, ±5V ranges). 4 microseconds max. for ±10V range.
Settling Time (1 LSB step)	1 microsecond to ±0.01%
Slew Rate	10 V/µSec min.
DIGITAL INPUT/OUTPUT	
Number of Lines	4 inputs, 3 outputs, non-isolated
Logic Levels	Compatible with TTL, TTL-LS, ALS, etc. Inputs: "0" (0.8V, "1") 2.0V Outputs: "0" (0.4V, "1") 2.4V
I/O Loading	Inputs: 1 LS load plus 10 Kilohm pullup to +5V. Outputs: 24 mA source or sink
COUNTER/TIMER	
Function	Used as an update strobe for each multichannel DAC frame.
Frequency Range	2 MHz to 536.87 seconds (32-stage binary or BCD divider).
Frequency Stability	±50 ppm/ °C
Spare Counter	16-stage binary divider usable for any purpose. Will divide input signals from 2 to 65,535. Includes counter input and output, 1 TTL-LS load, 10 MHz max input.

VME BUS INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Architecture	Memory mapped in 8 contiguous word locations on 256-byte boundaries. SAD24:SD16 slave.
Memory Mapping	Decodes memory address lines A8 through A23 plus six address modifiers, AM5-AM0.
Address Modifier Codes	39h or 3Dh, selectable
Data Bus	16-bit transfer using VMEbus SYSCLK signal to generate DTACK* with selectable delay.
Trigger Interrupt	1 interrupt, selectable on IRQ 1-7 plus maskable programmable 8-bit vector ID.
MISCELLANEOUS	
Analog Section Adjustments	Full scale gain and zero or offset potentiometers are provided for each DAC channel. See note 2.
Analog Connector [P1]	25-pin DB-25S, also includes the external trigger input.
Digital I/O Connector [P2]	9-pin DB-9S
Operating Temp Range	0 to +60 °C
Storage Temp Range	-25 to +85 °C
Relative Humidity	10% to 90%, non-condensing
Altitude	0 to 10,000 feet (0-3048 m). Forced cooling is recommended.
Power Supply Requirements	+5V dc, ±5% supplied from VME bus. 2.5 Amps typ., 4.0 Amps max. (16 channels), 1.5 Amps typ., 2.5 Amps max. (8 channels).
Outline Dimensions	Double height 6U VME outline.
Weight	1.5 pounds (0,7 Kg)

Notes

1. Depending on the host computer, block transfers may occur over 1 megasample per second and will accept a host DMA controller for the highest speed. When estimating system timing, account for any remaining interrupts required (such as the real time clock) and DRAM refresh delays, if any.

2. Recalibration is recommended at 90 day intervals, depending on conditions.

3. All DAC input registers reset to zero or half-scale (0800h) at power-up or bus reset, depending on the unipolar/bipolar switch selection.

REGISTER MEMORY MAPPING

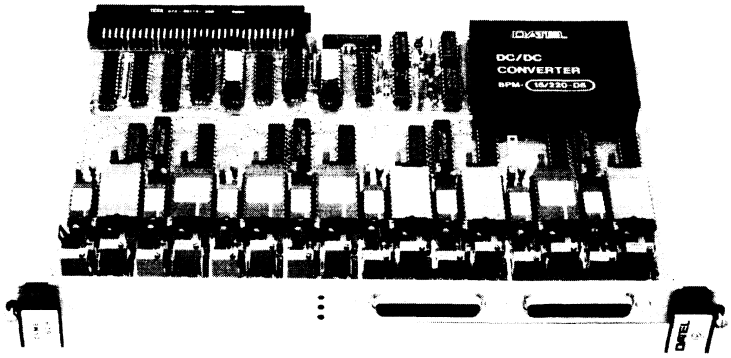
At power-up or VME bus reset, all control registers contain zeroes. The DAC data register should be programmed after setting up the channel address and command mode. The 82C54 registers must be programmed in a specific sequence, discussed in the user manual. 16-bit word instructions must be used. Unlisted registers are not used.

Address (hex)	Direction	Description
BASE + 0	Write	Command and Vector ID Register
BASE + 0	Read	Status and digital input Register
BASE + 2	Write	DAC Channel Address Register
BASE + 4	Write	DAC Data Register
BASE + 6	Write	Simultaneous Update Register
BASE + 8	Read/Write	Counter 0 (82C54)
BASE + 0Ah	Read/Write	Counter 1 (82C54)
BASE + 0Ch	Read/Write	Counter 2 (82C54)
BASE + 0Eh	Read/Write	Control Word Register (82C54)

DVME-628
12-Bit, 8-Channel VMEbus D/A Board

FEATURES

- **8 D/A channels**
- **12-Bit resolution**
- **Complete hardware-compatible with VMEbus specifications.**
- **6 μSecond settling time.**
- **Three types of input coding:**
  - **A. Bipolar 2's complement**
  - **B. Bipolar offset binary**
  - **C. Unipolar straight binary**
- **Five output voltage ranges:**
  - **A. 0 to +5V dc**
  - **B. 0 to +10V dc**
  - **C. ±2.5V dc**
  - **D. ±5V dc**
  - **E. ±10V dc**
- **Up to 0.05% full-scale range accuracy.**
- **±1/2 LSB differential nonlinearity**
- **4-to-20 mA current loop output capability for DVME-628C model.**
- **On-board dc-to-dc power converter supplies ±15V dc for internal logic circuits.**



THE DVME-628 IS DATEL's HIGH-END, VMEbus-BASED D/A BOARD THAT PROVIDES ANALOG OUTPUT FOR UP TO 8 CHANNELS. THE 12-BIT D/A BOARD, WITH 6 MICROSECOND SETTLING TIME, IS DESIGNED TO DELIVER HIGH-PERFORMANCE IN PROCESS CONTROL, TEST INSTRUMENTATION AND SIMILAR APPLICATIONS. THE THREE INPUT CODING SCHEMES AND FIVE ANALOG OUTPUT VOLTAGE RANGES MAKES THE BOARD AN IDEAL CHOICE FOR MOST INDUSTRIAL APPLICATIONS.

GENERAL DESCRIPTION

DATEL's VMEbus family of boards offer a complete solution to various data acquisition applications. The DVME-628 is the D/A member of this family, providing up to 8 analog outputs for the host VMEbus system. The D/A board offers a resolution of 12 bits and operates with an accuracy of beter than 0.05% of full-scale range. The board is rigorously tested under extreme environmental conditions for DATEL's stringent quality assurance requirements.

The DVME-628 easily fits into a VMEbus card cage and is addressable using short I/O space address lines. The on-board switches select the base address of the board. Functions relating to input data coding and output voltage range are easily selectable using jumpers.

Functionally, the DVME-628 consists of a VMEbus interface section and a digital-to-analog conveter (DAC) section. The DAC data register section contains a data register and D/A converter for each section. For DVME-628C models the DAC section also contains voltage to 4-to-20 mA current loop conversion logic for each channel. One unique feature of the DVME-628 is that the DAC outputs will reset to 0.000V during reset regardless of whether unipolar or bipolar outputs are selected.

The DVME-628 D/A board will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the board. The user's manual also contains information on troubleshooting the board.

The board is shipped with an example 68010 assembly language diagnostic program on a 5 1/4" floppy diskette, formatted using VERSAdos. The diagnostic program source code is available in hard copy from DATEL. Consult the factory regarding the availability of the diagnostic program's source code in other disk formats.

ORDERING INFORMATION

DVME-628 [V - Voltage outputs only; C - Voltage and 4-to-20mA current loop outputs]

VMEbus Interface

The DVME-628 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-628 generates the data acknowledge (DTACK★) signal to notify acceptance of data from the VMEbus data lines, D00 through D15. The DTACK★ signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.
The interface logic decodes the VMEbus control lines WRITE ★, DS0 ★, DS1 ★, and AS ★ to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-628 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

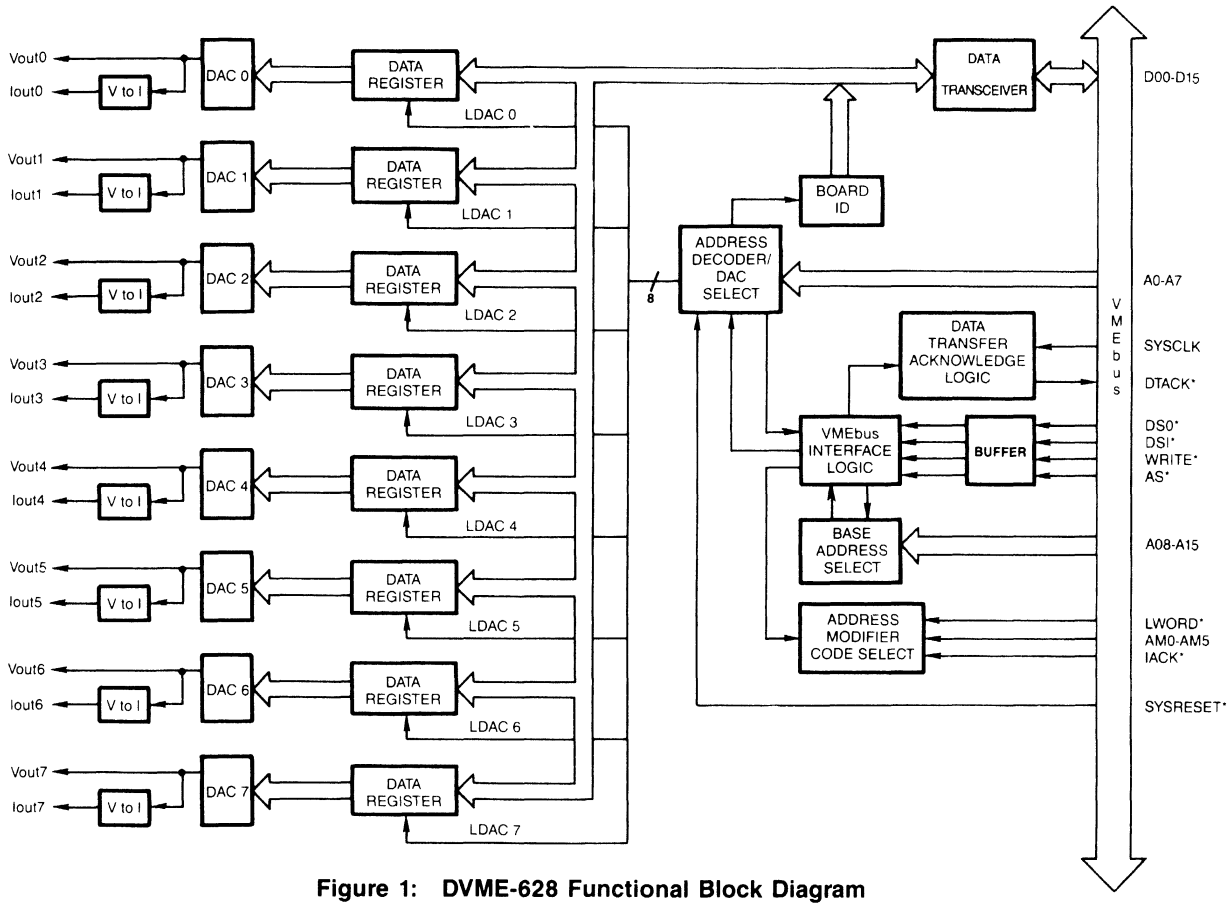


Figure 1: DVME-628 Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, unless otherwise noted)

Interface specifications

Data Bus.....16 Bits (A16:D16 slave)

Address Bus.....Short I/O Space; 16 address lines

Address Modifier Codes.....Codes used 29H, 2DH, 39H, and 3DH

Memory Mapping.....Short I/O space, user or supervisor, 256 words allocated per board

Data Transfer.....DTACK ★ signal line. Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector.....96-pin male DIN connector

J1 and J2 Analog Output Connectors....25-pin D-type female connector.

ANALOG SPECIFICATONS

ANALOG OUTPUT

Number of Channels..... 8 non-isolated, single-ended

Output Range.....0 to +5V dc
0 to +10V dc
± 2.5V dc
± 5V dc
± 10V dc

Digital Input Coding.....Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary

NOTE: The VMEbus SYSCLK signal is required.

Resolution . . . . . 12 Bits

Reset . . . . . Output resets to 0.000V dc at power-on

Accuracy . . . . . 0.05% of FSR, minimum

Differential . . . . . 0.5 LSB, maximum non-linearity

Zero Temperature Drift . . . . . 3 ppm/ °C, typical
5 ppm/ °C, maximum

Offset Temperature Drift . . . . . 5 ppm/ °C, typical
10 ppm/ °C, maximum

Gain Temperature Drift . . . . . 15 ppm/ °C, typical
30 ppm/ °C, maximum

Settling Time . . . . . 6 μSeconds, maximum

Output Current . . . . . ±5 mA, typical

Output Impedance . . . . . 50 milliohms, typical

CURRENT LOOP

Current Loop . . . . . 4-to-20 mA, conforming to ISA Standard 550.1, Type 4, Class U

Accuracy . . . . . 0.1% of FSR, minimum

Excitation . . . . . +15V dc, minimum
(User-supplied) . . . . . +24V dc, typical
+36V dc, maximum

Load Resistance . . . . . 100 Ohms, minimum
1000 Ohms, maximum

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at . . . . . 2.0 Amperes, typical
2.3 Amperes, maximum

PHYSICAL CHARACTERISTICS

Outline Dimensions . . . . . 9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)

Weight . . . . . 1 lb. (453.6 grams)

Operating Temperature Range . . . . . 0 to +60 °C

Storage Temperature Range . . . . . -20 to +80 °C

Humidity . . . . . 0 to 90%, non-condensing

DVME-628 PROGRAMMING INFORMATION

The DVME-628 contains eight programmable registers that store digital data for the D/A converters. The board responds only to word data transfers on write operations. Since the DVME-628 uses 12-bit D/A converters, the 12 most significant bits of the DAC data registers are used for conversion. Table 1 shows the addresses of the identification code and the registers. Figure 2 shows the format of the DAC data register.

Table 1: DVME-628 Register Locations

ADDRESS	FUNCTION	CONTENTS
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 160	Write	D/A Channel 0
Base + 162	Write	D/A Channel 1
Base + 164	Write	D/A Channel 2
Base + 166	Write	D/A Channel 3
Base + 168	Write	D/A Channel 4
Base + 170	Write	D/A Channel 5
Base + 172	Write	D/A Channel 6
Base + 174	Write	D/A Channel 7

Word Address: Base + 160, Base + 162, Base + 164, Base + 166, Base + 168, Base + 170, Base + 172, and Base + 174

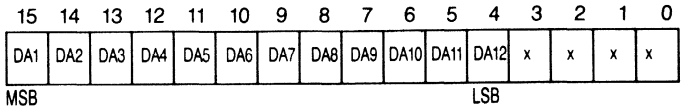


Figure 2: DVME-628 DAC Data Register Format

OUTPUT CONNECTIONS

The DVME-628 D/A boards use the J1 and J2 connectors for analog output connections. Tables 2 and 3 list the output signals of the J1 and J2 connector respectively.

Table 2: DVME-628 Analog Output Pinout Details (J1)

PIN #	DESCRIPTION
1	DAC 0 V OUT
2	DAC 0 I LOOP
3	DAC 0 V LOOP
4	DAC 1 V OUT
5	DAC 1 I LOOP
6	DAC 1 V LOOP
7	DAC 2 V OUT
8	DAC 2 I LOOP
9	DAC 2 V LOOP
10	DAC 3 V OUT
11	DAC 3 I LOOP
12	DAC 3 V LOOP
13	NO CONNECTION
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	NO CONNECTION
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	NO CONNECTION
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	NO CONNECTION
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	NO CONNECTION

Table 3: DVME-628 Analog Output Pinout Details (J2)

PIN #	DESCRIPTION
1	DAC 4 V OUT
2	DAC 4 I LOOP
3	DAC 4 V LOOP
4	DAC 5 V OUT
5	DAC 5 I LOOP
6	DAC 5 V LOOP
7	DAC 6 V OUT
8	DAC 6 I LOOP
9	DAC 6 V LOOP
10	DAC 7 V OUT
11	DAC 7 I LOOP
12	DAC 7 V LOOP
13	NO CONNECTION
14	DAC 4 ANALOG RETURN
15	DAC 4 ANALOG RETURN
16	NO CONNECTION
17	DAC 5 ANALOG RETURN
18	DAC 5 ANALOG RETURN
19	NO CONNECTION
20	DAC 6 ANALOG RETURN
21	DAC 6 ANALOG RETURN
22	NO CONNECTION
23	DAC 7 ANALOG RETURN
24	DAC 7 ANALOG RETURN
25	NO CONNECTION

DVME-628 BOARD IDENTIFICATION CODE

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	2	
+ 1F	8	

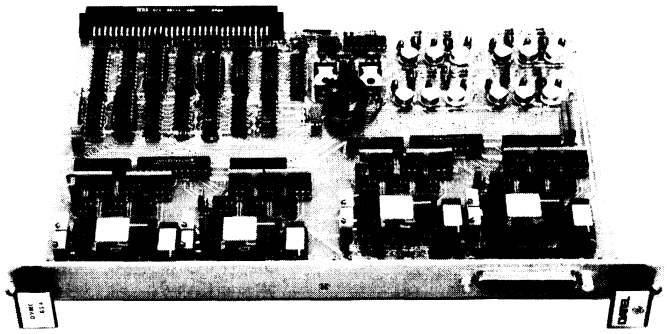
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

DVME-624
Isolated 4-Channel, 12-Bit, VMEbus D/A Board

FEATURES

- **4-Channel memory mapped D/A board**
- **300 VRMS channel-to-channel and channel-to-bus isolation**
- **Hardware compatible with VMEbus specifications**
- **On-board isolated dc-to-dc power converter**
- **Optional 6 μS or 30 μS settling time models**
- **12-Bit resolution**
- **Choice of output voltages:**
  - **a. 0 to 5V dc**
  - **b. 0 to 10V dc**
  - **c. ±2.5V dc**
  - **d. ±5V dc**
  - **e. ±10V dc**
- **Optional 4-to-20mA current loop capability conforming to ISA standards**
- **±1/2 LSB differential non-linearity**
- **±0.05% Full-scale range accuracy**



GENERAL DESCRIPTION

The DVME-624 is DATEL's 12 bit, 4 channel D/A board, totally compatible with VMEbus specifications. In a typical application the board provides analog outputs in real-time to the host system at a high speed. The different full-scale output voltage ranges the board offers conform to process control and test and measurement industrial requirements.

Each channel is configurable to different output voltage ranges. The salient feature of the DVME-624 board is the 300 VRMS channel-to-channel and channel-to-bus isolation. The board uses high performance optoisolators to provide the isolation. An on-board dc-to-dc power converter provides isolated power to each D/A converter section.

The isolation makes the DVME-624 an ideal choice for applications where a low-level signal superimposes a high voltage such as in testing of power supplies. The channel-to-bus isolation protects the host system against any catastrophic damages due to an external malfunction such as an actuator failure.

The DVME-624 offers ±1/2 LSB differential non-linearity and operates at ±0.05% full-scale range accuracy. The DVME-624 models are available at two different settling times. The lower cost DVME-624C1 and DVME-624V1 models offer 30 μS settling time and the DVME-624C2 and DVME-624V2 models offer 6 μS settling time. The DVME-624 may be obtained with an optional 4-to-20mA industrial current loop output in addition to the voltage outputs. Refer to the ordering information for models with current loop option.

Functionally, the digital data from the VME host system is transferred through a 12-bit data register to one-of-four D/A sections. The DVME-624 converts the 12 most significant bits from the VME data bus to an analog output. Data from the host system may be in straight binary, offset binary, or 2's complement coding. The D/A converter sections are optically isolated from the VME interface logic. The DVME-624 uses monolithic D/A converters to increase the product's reliability and endurance.

The DVME-624 D/A boards will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the DVME-624. The DVME-624 is shipped with an 68010 assembly language diagnostic program example on a 5 1/4" MS-DOS formatted diskette. The diagnostic program's source code is available in hardcopy from DATEL.

ORDERING INFORMATION

DVME-624

- 1 — 30 μS Settling time
- 2 — 6 μS Settling time
- V — Voltage output only
- C — Voltage and 4-to-20 mA current loop output

VME Interface

The DVME-624 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to the address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-624 generates the data acknowledge (DTACK*) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK* signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems. Figure 1 shows the functional block diagram of the DVME-624 D/A board.

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, V_{exc} = +24V dc, R_{loop} = 250 ohms, unless otherwise specified.)

INTERFACE SPECIFICATIONS

Data Bus	16 bits
Address Bus	Short I/O Space, 16 address lines
Address modifiers codes	Codes used 29H, 2DH, 39H, and 3DH
Memory Mapping	Short I/O space, user or supervisor 256 bytes allocated per board (A16:D16 slave).

INTERNAL HARDWARE REGISTER/SOFTWARE ASSIGNMENTS

Register Memory Mapping

Relative Address	Function	READ/WRITE
0 through 63	Board Identification Code	Read Only
64 through 127	See Note 1	Read Only
128 through 159	See Note 2	Write Only
160	D/A Channel 0	Write Only
162	D/A Channel 1	Write Only
164	D/A Channel 2	Write Only
166	D/A Channel 3	Write Only
168 through 255	See Note 2	Write Only

Note 1: These addresses are redundant with ID PROM addresses, base + 0 through base + 63.

Note 2: These addresses are redundant in 8-byte blocks with the DAC data registers, base + 160 through base + 166.

The VMEbus SYSCLK signal is required.

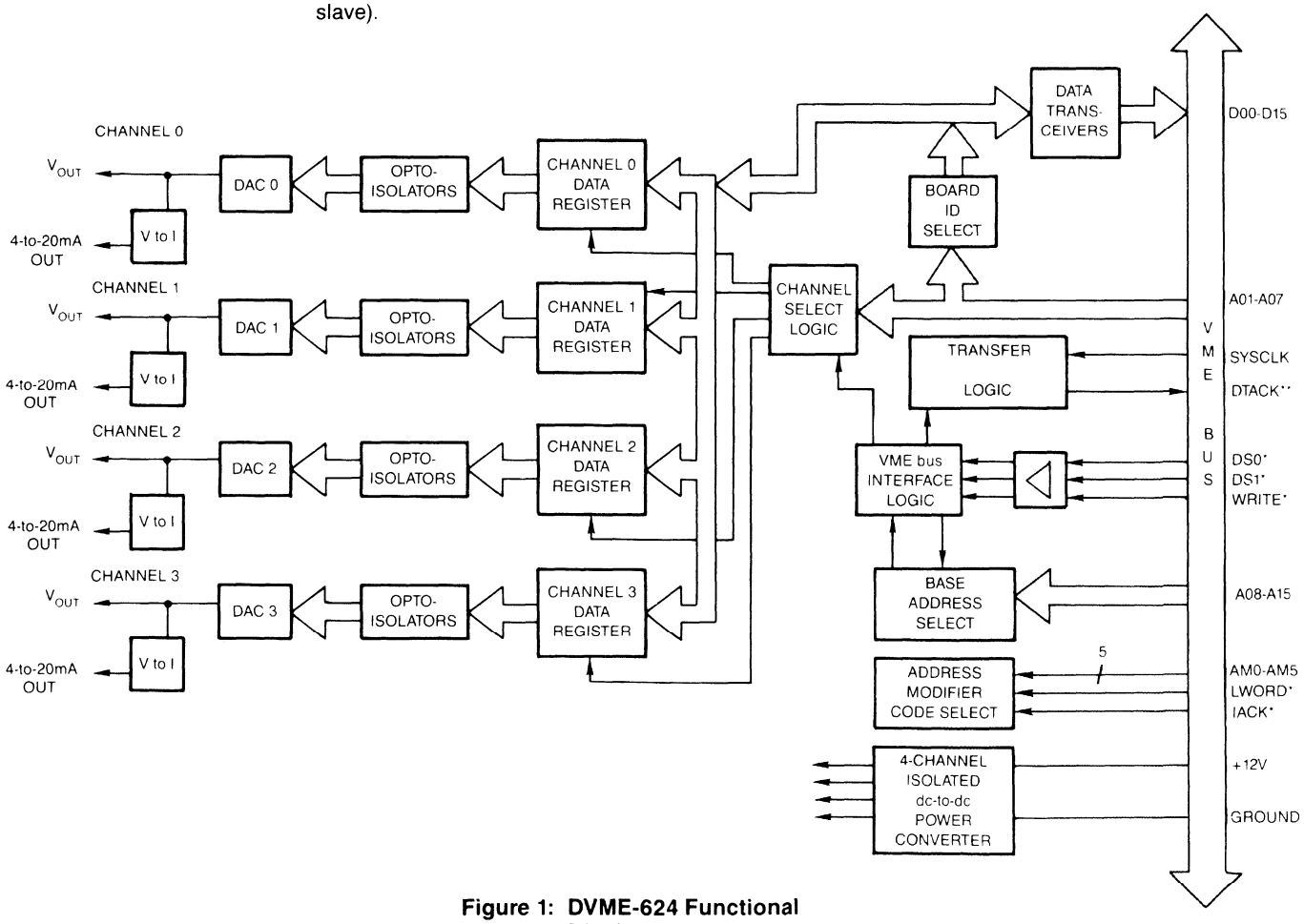


Figure 1: DVME-624 Functional Block Diagram

CONNECTOR SPECIFICATIONS

VME bus — P1 . . . . . 96-pin male DIN connector

Analog Output — J1 . . . . . 25-pin D Type female connector, Amp P/N 745783-1 or equivalent

ANALOG OUTPUT SPECIFICATONS

Number of Channels 4

Channel-to-channel Isolation . . . . . 300 VRMS, sustained maximum

Output full-scale voltage ranges (Selectable per channel) . . . . . 0 to 5V dc
0 to 10V dc
±2.5V dc
±5V dc
±10V dc (standard)

Input data coding . . . . . Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary

Resolution . . . . . 12 Bits. Uses 12 most significant data bits from the data bus. Ignores bits D0 through D3.

Reset . . . . . Minus full-scale, output resets to 0.000V dc

Current Loop . . . . . 4-to-20 mA. Meets ISA standard 550.1 Type 4 Class U

Excitation Voltage (User-supplied) . . . . . 15 to 36V dc

PERFORMANCE

Specification	Minimum	Typical	Maximum
Accuracy	0.05% of FSR	—	—
Differential non-linearity	—	—	0.5 LSB
Zero temperature drift	—	3 ppm/°C	5 ppm/°C
Offset temperature	—	5 ppm/°C	10 ppm/°C
Gain temp drift	—	15 ppm/°C	30 ppm/°C
Settling time:			
DVME-624V1 DVME-624C1	—	—	30 μseconds
DVME-624V2 DVME-624C2	—	—	6 μseconds
Output current	—	±5 mA	—
Output impedance	—	50 milliohms	—

Note: The 6 microsecond option should be selected for low transient applications such as amplifier inputs.

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1.0A typical, 1.2A maximum

+12V dc ±2.0% at 0.4A typical, .7A maximum

CURRENT LOOP

Specification	Minimum	Maximum
Accuracy	0.1% of FSR	—
Excitation (user-supplied)	15V dc	36V dc
Load resistance	100 Ohms	1000 Ohms
Isolation channel-to-channel	300 VRMS	—
Isolation output-to-bus	300 VRMS	—

PHYSICAL CHARACTERISTICS

Outline Dimensions . . . . . 9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)

Weight . . . . . 9.6 oz (272.3 grams)

Operating temperature range . . . . . 0 to 60°C

Storage temperature range . . . . . −20 to +80°C

Relative humidity . . . . . 0 to 90%, non-condensing

DVME-624 ANALOG OUTPUT CONNECTOR J1

The DVME-624 provides analog outputs using the J1 connector. Depending on the model, the J1 connector contains voltage and current loop outputs. Figure 2 shows the output signals on the J1 connector.

PIN NUMBER	DESCRIPTION
1	DAC 0 V OUT
2	DAC 0 I LOOP
3	DAC 0 V LOOP
4	DAC 1 V OUT
5	DAC 1 I LOOP
6	DAC 1 V LOOP
7	DAC 2 V OUT
8	DAC 2 I LOOP
9	DAC 2 V LOOP
10	DAC 3 V OUT
11	DAC 3 I LOOP
12	DAC 3 V LOOP
13	
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	

Figure 2: Analog output pinout details

DVME-624 DATA FORMAT

The DVME-624 uses a 12-bit D/A converter for converting the digital data to analog signal. The board uses the 12 most significant bits of the VME data lines as input signals. Figure 3 shows the data format the DVME-624 is designed for.

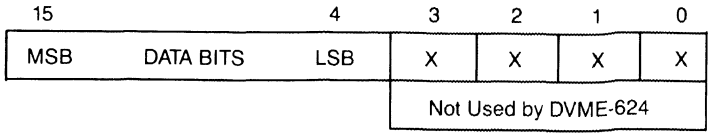


Figure 3: DVME-624 data format

DVME-624 Board Identification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	2	
+ 1F	4	

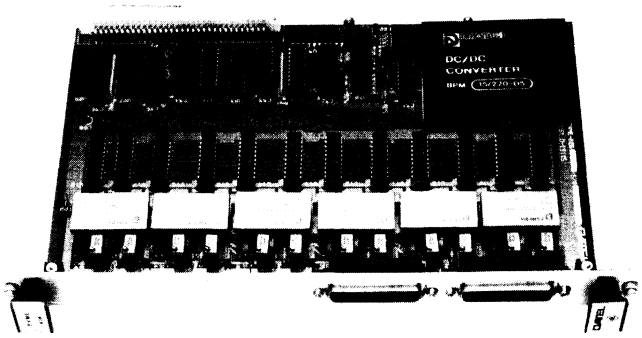
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

DVME-626
16-Bit, 6-Channel VMEbus D/A Board

FEATURES

- 6 D/A channels
- 16-Bit resolution
- 14-Bit monotonicity
- Designed to meet precision servo control requirements
- Complete hardware-compatible with VMEbus specifications
- 15 μSecond settling time
- Available in two models:
  DVME-626V1 for ±10V dc output
  DVME-626V2 for 0 to +10V dc and ±5V dc outputs
- Three input coding types:
  A. Bipolar 2's complement
  B. Bipolar offset binary
  C. Unipolar straight binary
- Up to 0.005% full-scale range accuracy
- ±0.005% of full-scale range differential nonlinearity
- On-board dc-to-dc power converter supplies ±15V dc for internal logic circuits



The DVME-626 is DATEL's high resolution VMEbus-based D/A board that provides analog outputs for up to 6 channels. The 16-bit D/A board is designed to deliver exceptionally high-performance in rugged industrial environments. The 14-bit monotonicity and 0.005% FSR accuracy makes the board an ideal choice for precision servo control and similiar applications. The DVME-626 is supported by MS-DOS software for calibration and diagnostics.

GENERAL DESCRIPTION

The DVME-626 is a D/A member of DATEL's VMEbus family. The board delivers precision and performance that makes it easily acceptable for various test and control applications. On-board hardware resources provide 6 high-resolution analog outputs with an accuracy of better than 0.005% of full-scale range. The DVME-626 accepts 16-bit digital data, coded in bipolar 2's complement, bipolar offset binary, or unipolar straight binary. The board is rigorously tested under extreme environmental conditions to meet DATEL's stringent quality assurance requirements.

The DVME-626 easily fits into a VMEbus card cage and is addressable using short I/O space address lines. The on-board switches select the base address of the board. Functions relating to input data coding and output voltage range are easily selectable using jumpers.

Functionally, the DVME-626 consists of a VMEbus interface section and a digital-to-analog converter (DAC) section. The DAC data register section contains a data register and D/A converter for each section. One unique feature of the DVME-626 is that the DAC outputs will reset to 0.000V during reset, regardless of whether unipolar or bipolar outputs are selected. Figure 1 shows the functional block diagram of the board.

The DVME-626 D/A board will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the board. The user's manual also contains information on troubleshooting the board.

The board is shipped with an example 68010 assembly language diagnostic program on a 5 1/4" floppy diskette, formatted for the MS-DOS operating systems. Consult the factory regarding the availability of the diagnostic program's source code on other disk formats.

ORDERING INFORMATION

DVME-626V
- 1 — ± 10V dc output range
- 2 — 0 to 10V and ±5V dc output ranges

VMEbus Interface

The DVME-626 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-626 generates the data acknowledge (DTACK ⋆) signal to notify acceptance of data from the VMEbus data lines, D00 through D15. The DTACK ⋆ signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host CPU response times.

The interface logic decodes the VMEbus control lines WRITE ⋆, DS0 ⋆, DS1 ⋆, and SYSRESET ⋆ to select and control the interface. These signals control the board select and the VMEbus transfer functions. The DVME-626 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

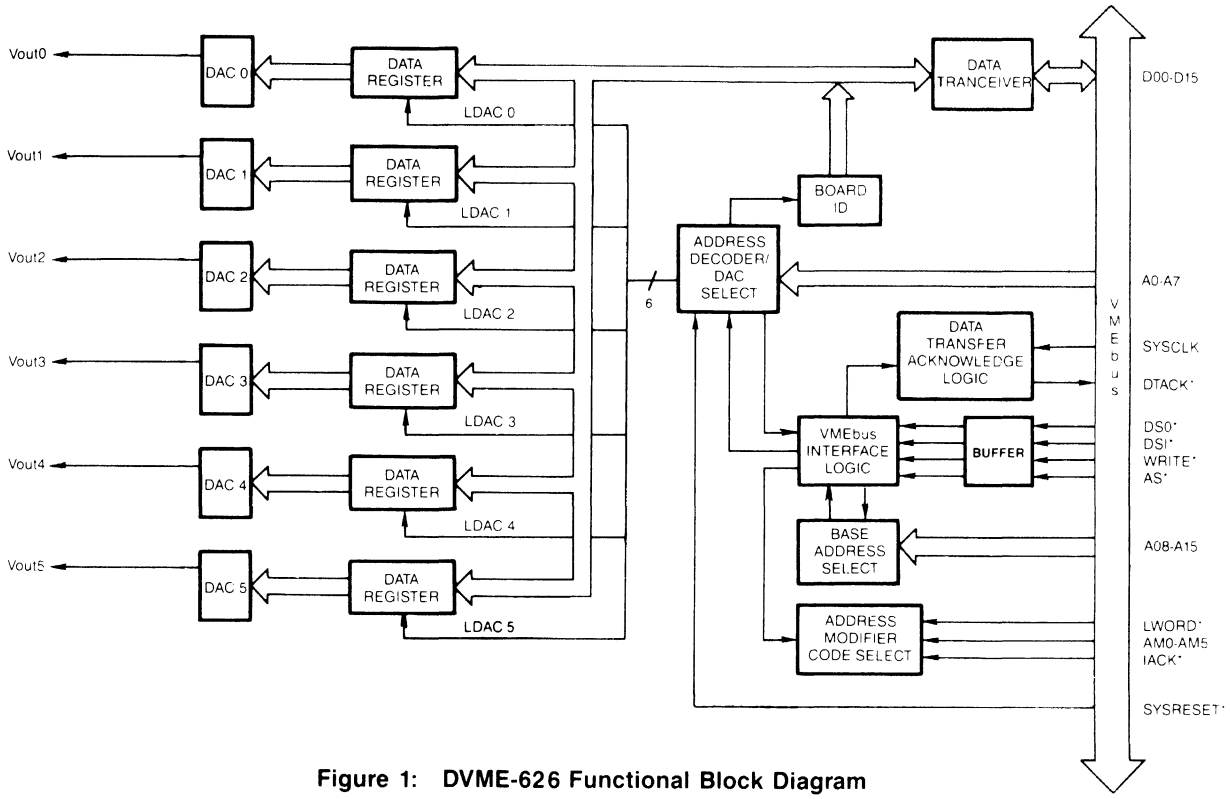


Figure 1: DVME-626 Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, unless otherwise noted)

INTERFACE SPECIFICATIONS

Data Bus.....16 Bits (A16:D16 slave)

Address Bus.....Short I/O Space; 16 address lines

Address Modifier Codes.....Codes used 29H, 2DH, 39H, and 3DH

Memory Mapping.....Short I/O space, user or supervisor, 256 words allocated per board.

Data Transfer.....DTACK ⋆ signal line. Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines.

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector.....96-pin male DIN connector.

J1 and J2 Analog Output Connectors.....25-pin D-type female connector, DB-25S

ANALOG SPECIFICATONS

ANALOG OUTPUT

Number of Channels.....6, non-isolated

Output Range
DVME-626V1.....±10V dc
DVME-626V2.....0 to 10V and ± 5V dc

Digital Input Coding.....Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary
(jumperable)

Note: The VMEbus SYSCLK signal is required.

Resolution . . . . . 16 Bits

Monotonicity . . . . . 14 bits

Reset . . . . . Output resets to 0.000V dc at power-on

Accuracy . . . . . 0.005% of FSR, minimum

Differential nonlinearity . . . . . 0.005% of FSR, maximum

Zero temperature drift . . . . . 5 ppm/°C, typical

Offset temperature drift . . . . . 8 ppm/°C, typical

Gain temperature drift . . . . . 20 ppm/°C, typical

Settling time . . . . . 15 μseconds (small step)

Output current . . . . . ±5 mA, typical

Output impedance . . . . . 50 milliohms, typical

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 3.0 Amperes, typical

Power Supply Rejection . . . . . ±0.002%, typical

PHYSICAL CHARACTERISTICS

Outline Dimensions . . . . . 9.19″ W×6.3″ D×0.6″ H (233.35×160×15.24 mm)

Weight . . . . . 1 lb. (453.6 grams)

Operating Temperature Range . . . . . 0 to +60° C Range

Storage Temperature Range . . . . . −20 to +80° C Range

Humidity . . . . . 0 to 90%, non-condensing

DVME-626 PROGRAMMING INFORMATION

The DVME-626 contains six programmable registers that store digital data for each 16-bit D/A converter. The board responds only to word data transfers on write operations. Table 1 shows the addresses of the identification code and the registers. Figure 2 shows the format of the DAC data register.

Table 1: DVME-626 Register Locations.

ADDRESS	FUNCTION	CONTENTS
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 160	Write	D/A Channel 0
Base + 162	Write	D/A Channel 1
Base + 164	Write	D/A Channel 2
Base + 166	Write	D/A Channel 3
Base + 168	Write	D/A Channel 4
Base + 170	Write	D/A Channel 5

Word Address: Base + 160, Base+162, Base+164, Base+166, Base + 168, and Base + 170

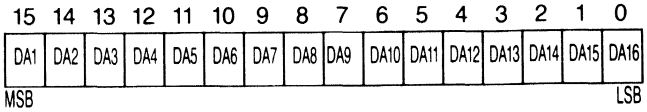


Figure 2: DVME-626 DAC Data Register Format

I/O CONNECTIONS

The DVME-626 D/A boards provide front panel J1 and J2 connectors for analog output connections. Tables 2 and 3 list the output signals of the J1 and J2 connectors respectively.

Table 2: DVME-626 ANALOG OUTPUT CONNECTOR J1

PIN #	DESCRIPTION
1	DAC 0 V OUT
2	NO CONNECTION
3	NO CONNECTION
4	DAC 1 V OUT
5	NO CONNECTION
6	NO CONNECTION
7	DAC 2 V OUT
8	NO CONNECTION
9	NO CONNECTION
10	DAC 3 V OUT
11	NO CONNECTION
12	NO CONNECTION
13	NO CONNECTION
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	NO CONNECTION
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	NO CONNECTION
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	NO CONNECTION
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	NO CONNECTION

Table 3: DVME-626 ANALOG OUTPUT CONNECTOR J2

PIN #	DESCRIPTION
1	DAC 4 V OUT
2	NO CONNECTION
3	NO CONNECTION
4	DAC 5 V OUT
5	NO CONNECTION
6	NO CONNECTION
7	NO CONNECTION
8	NO CONNECTION
9	NO CONNECTION
10	NO CONNECTION
11	NO CONNECTION
12	NO CONNECTION
13	NO CONNECTION
14	DAC 4 ANALOG RETURN
15	DAC 4 ANALOG RETURN
16	NO CONNECTION
17	DAC 5 ANALOG RETURN
18	DAC 5 ANALOG RETURN
19	NO CONNECTION
20	NO CONNECTION
21	NO CONNECTION
22	NO CONNECTION
23	NO CONNECTION
24	NO CONNECTION
25	NO CONNECTION

DVME-626 Board Identification Code

Byte Address	ASCII Code	FUNCTION
Base + 1 Base + 3 Base + 5 Base + 7 Base + 9	V M E I D	Identifier. This ASCII code is present for all DATEL VMEbus boards
Base + 0B Base + 0D Base + 0F	D A T	Manufacturer ID. DAT is the ID for DATEL
Base + 11 Base + 13 Base + 15 Base + 17 Base + 19 Base + 1B Base + 1D Base + 1F	d V M E – 6 2 6	Board model number

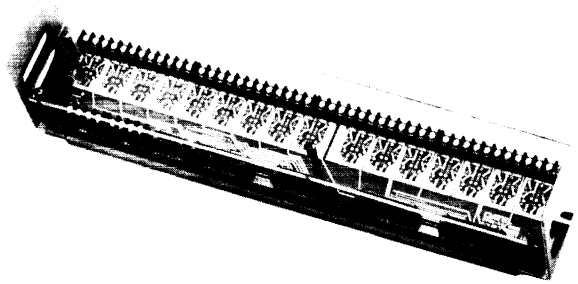
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base+0 through Base+63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base+64 through Base+77	DVME-660	48 line digital I/O board
Base+78 through Base+127	----------	Not Used ----------
Base+128 through Base+143	DVME-611	DVME-611: 32 single-ended/ 16 differential channel A/D board
	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base+144 through Base+151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples, RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base+152 through Base+159	----------	Not Used ----------
Base+160 through Base+175	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
	DVME-624	DVME-624: 4-channel isolated board
	DVME-626	DVME-626: 6-channel 16-bit D/A board
	DVME-628	DVME-628: 8-channel 12-bit D/A board
Base+176 through Base+191	----------	Not Used ----------
Base+192 through Base+255	----------	Not Used ----------

DVME-691A and -691D
Rack-mounted, Signal-Conditioning Screw Terminator Panel

FEATURES

- **Rack-mounted screw-terminations for factory wiring**
- **Two models available:**
  DVME-691A for analog inputs
  DVME-691D for analog outputs
- **Both versions have component etch wiring ready to accept discrete components for signal conditioning**
- **DVME-691A Version includes component pads for shunts, attenuators, filters, and spike clamps**
- **DVME-691D Version includes component pads for current loop excitation**
- **DVME-691A handles up to 32 single-ended inputs**
- **DVME-691D provides up to eight analog output channels**
- **Designed for 19 inch RETMA racks**
- **Complete with mounting hardware and cables**
- **Plexiglas safety shield for connector labeling**



THE DVME-691A AND DVME-691D TERMINATION PANELS OFFER A CONVENIENT WAY OF INTERFACING FIELD WIRING TO DATEL'S LINE OF VMEbus BOARDS. IN ADDITION, THE PANELS ARE DESIGNED TO INCORPORATE DISCRETE SIGNAL CONDITIONING COMPONENTS FOR EITHER ANALOG INPUTS OR OUTPUTS.

GENERAL DESCRIPTION

Offering a convenient method of connecting A/D or D/A channel wiring through screw terminators, the DVME-691 rack-mount interface panel is ideal for industrial and process control analog I/O connections. Field cabling need no longer be brought directly to the I/O connectors of the VMEbus boards. Instead, the user terminates all field wiring at the panel then uses DATEL's ribbon cabling system to bring signals to the specific boards.

The 3.5-inch high panel mounts into a standard RETMA 19" rack, letting the unit mount directly in the same rack as the user's VMEbus cardcage. All interwiring consists of flat ribbon cables, affording a quick disconnect capability.

Both versions interface I/O channels of DATEL's VMEbus boards to the user's field wiring using dedicated connectors, signal paths, and additional etch for user-installed discrete components. The DVME-691A can accommodate up to 32 single-ended or 16 differential analog input channels, plus two analog output channels. The DVME-691D accommodates up to eight analog output channels.

As supplied by the factory, signals pass from the screw terminals to specific flat ribbon connectors via etched circuitry. The user's sensor, transducer, and actuator cabling connects to screw terminals on the top portion of the DVME-691's. Prior to passing the signals on to the VMEbus cards, the user may introduce signal conditioning circuitry using the provided etch layout. The user solders in discrete components per the application requirements, cutting the etch (where necessary) which normally connects the input to the output connectors.

The DVME-691A and DVME-691D include five-foot-long flat cables used to pass the signals directly to DATEL's DVME-600 Series of high-performance VME A/D and D/A boards.

The mounting bracket, included in both versions, also has a Plexiglas safety shield which accommodates labeling requirements.

Two Versions for A/D or D/A

The DVME-691A and DVME-691D differ only in the placement and pinout of mating flat cable connectors. For analog inputs, model DVME-691A accepts up to 32 single-ended or 16 differential inputs, as supplied by DATEL's 32S/16D-channel DVME-611 or DVME-601 A/D board. The DVME-691A has two additional channels designated as analog output channels when using DATEL's DVME-612 combination A/D-D/A board.

For analog input channel expansion (up to 256 channels), the DVME-691A also works with DATEL's DVME-641 and DVME-645 slave analog input multiplexer channel expander boards. These expanders share the same A/D converter on the A/D master board, offering low channel costs and a simple means of adding more channels.

For analog outputs, Model DVME-691D distributes up to 8 D/A channels. The DVME-691D is directly compatible with DATEL's DVME-624, -626, -628 and -620 Series D/A boards.

Ordering Information
See Last Page

FUNCTIONAL SPECIFICATIONS

(Apply to the DVME-691A and DVME-691D unless otherwise noted.)

DVME-691A

Number of Analog Input Channels . . . . 32 single-ended or 16 differential plus 2 DVME-612 D/A channels.

Connections per Channel . . . . . Hi, Lo, Ground (Differential) and G,H,H,G,H,H, ... (Single-ended). Single-ended inputs share one ground for every two channels. There are 48 A/D terminals, total.

There are 4 screw terminals for the DVME-612 D/A outputs.

DVME-691D

Number of Analog Output Channels . . . 8 voltage outputs or current loops.

Connections per Channel . . . . . Voltage output, voltage return, current loop voltage, current loop output, current loop return. There are 5 terminals per D/A channel.

DVME-691A and DVME-691D

Screw Terminal Type . . . . . Barrier terminals using 6-32 screws on 0.325″ centers, suitable for lugs or bare wire, 16 gauge or smaller.

Mating Cables . . . . . Two 25-conductor flat cables are included to mate with DATEL's DVME-600 Series boards. The board end includes a DB-25P connector. The DVME-691 end includes a 26-pin self-keying flat cable header connector. Cable length is five feet.

The 691A also includes a five foot, 10-pin flat cable and DB-9P connector for the 2 DVME-612 D/A channels.

Front Safety Shield . . . . . 0.125″ thick Plexiglas shield accepts user terminal labelling. Remove shield for signal conditioning component installation.

Signal Conditioning . . . . . Component Pads accept user-supplied passive components for voltage attenuation, current shunt, RC filters, protective clamps, loop excitation, etc.

DC Power Rails . . . . . Bipolar DC power from a user-supplied power supply is distributed to all channels for loop excitation, clamps, etc. The rails are brought out to screw terminals for power supply connection.

Outline Dimensions . . . . . 19″ W x 3.5″ H x 4.62″ D with mounting slots on 3″ vertical centers and 18.5″ horizontal centers. (Suitable for 19″ RETMA rack mounting).

Operating Temperature . . . . . 0 to +70 degrees Celsius

COMPATIBILITY TABLE

TERMINATOR	USED WITH	TOTAL NUMBER OF CHANNELS
	Analog Inputs	
DVME-691A	**DVME-601**	16S or 8D A/D
DVME-691A	**DVME-611/612**	32S or 16D A/D plus 2 D/A
DVME-691A	**DVME-641**	32S or 16D Slave multiplexing A/D*
DVME-691A	**(2) DVME-645**	16S or 8D Simultaneous sample/hold*
	Analog Outputs	
DVME-691D	**(2) DVME-624**	8 Isolated D/A or 4-20 mA loop outputs
DVME-691D	**DVME-626**	6 High-resolution D/A
DVME-691D	**DVME-628**	8 D/A or 4-20 mA loop outputs

* (The slave MUX boards require a host DVME-611 or 612 A/D board).

DATEL's DVME-602 and DVME-643 boards include their own screw terminal interfaces and do not connect to the DVME-691.

Signal Conditioning Component Pads

DATEL ships the DVME-691 with straight-through connections between external devices and analog channels. However, the DVME-691 easily adapts to an extensive variety of signal conditioning circuits. Circuits consisting of passive components (resistors, capacitors, diodes, etc.) install directly on the 691's printed circuit board using etch provided.

The plated-through PC board pads are pre-drilled and clearly identified by screening labels. As configured, the pads support circuits for input attenuation, current shunt input (including 4-to-20 mA applications), noise filtering, and overvoltage protection clamps.

OUTLINE DIMENSIONS (TOP VIEW) IN (mm)

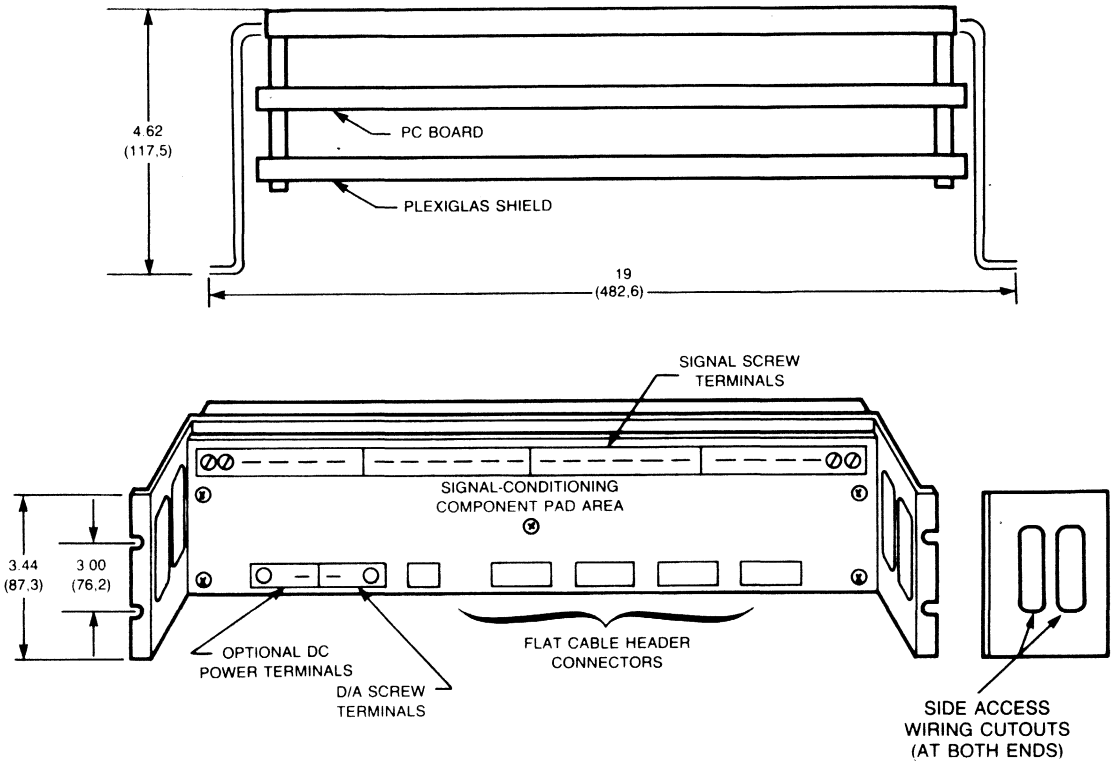


Figure 1. Connector Locations/Dimensions

DC Power Rails

Adjacent to each channel are bipolar dc power supply rails. These may be used for clamp circuits, for sensor excitation, or open-circuit detection. The dc rails are brought out to screw terminals suitable for connection to an adjacent dc power supply. There is ample room to mount a supply on standoffs on the rear of the DVME-691. Voltages up to ±15V dc may be distributed to each channel.

For D/A outputs, the signal conditioning pads could be used for excitation of 4-to-20 mA current loops. Such excitation circuits would use the dc power supply, the distributed dc rails, and current-excitation resistors on a per-channel basis.

Signal Conditioning Circuitry

Signal-conditioning circuitry can be of the user's design or DATEL can provide the design, testing, and installation of such circuitry under special quantity order.

Sensor Families

As configured, the DVME-691A is ideal for voltage and millivolt-input sources. These include bridges, strain gages, load cells, and RTD's. The DVME-691 adapts to 4-to-20 mA loop inputs by adding current loop shunts. The DVME-691A accepts thermocouple inputs if the user supplies external cold junction compensation (CJC).

Alternatively, electronic CJC may be provided on the A/D board by using DATEL's Model DVME-602T or DVME-643T slave thermocouple channel expander boards. These two products include their own front panel screw terminals.

OTHER FEATURES

The DVME-691 is intended for factory-floor, industrial, and laboratory applications. As shown in Figure 1, the screw terminals accept field signal wiring either as bare wire or terminated with strain-relieved lugs. Access holes in the sides of the DVME-691 permit routing the wiring through the rear of the DVME-691. Because of this access, several DVME-691's can mount above each other in the same rack or directly adjacent to the host A/D-D/A computer.

The DVME-691 also includes a transparent safety shield which prevents accidental contacts while providing a means of labelling each connection. The DVME-691 does not protrude from the rack.

TYPICAL RACK-MOUNT APPLICATION

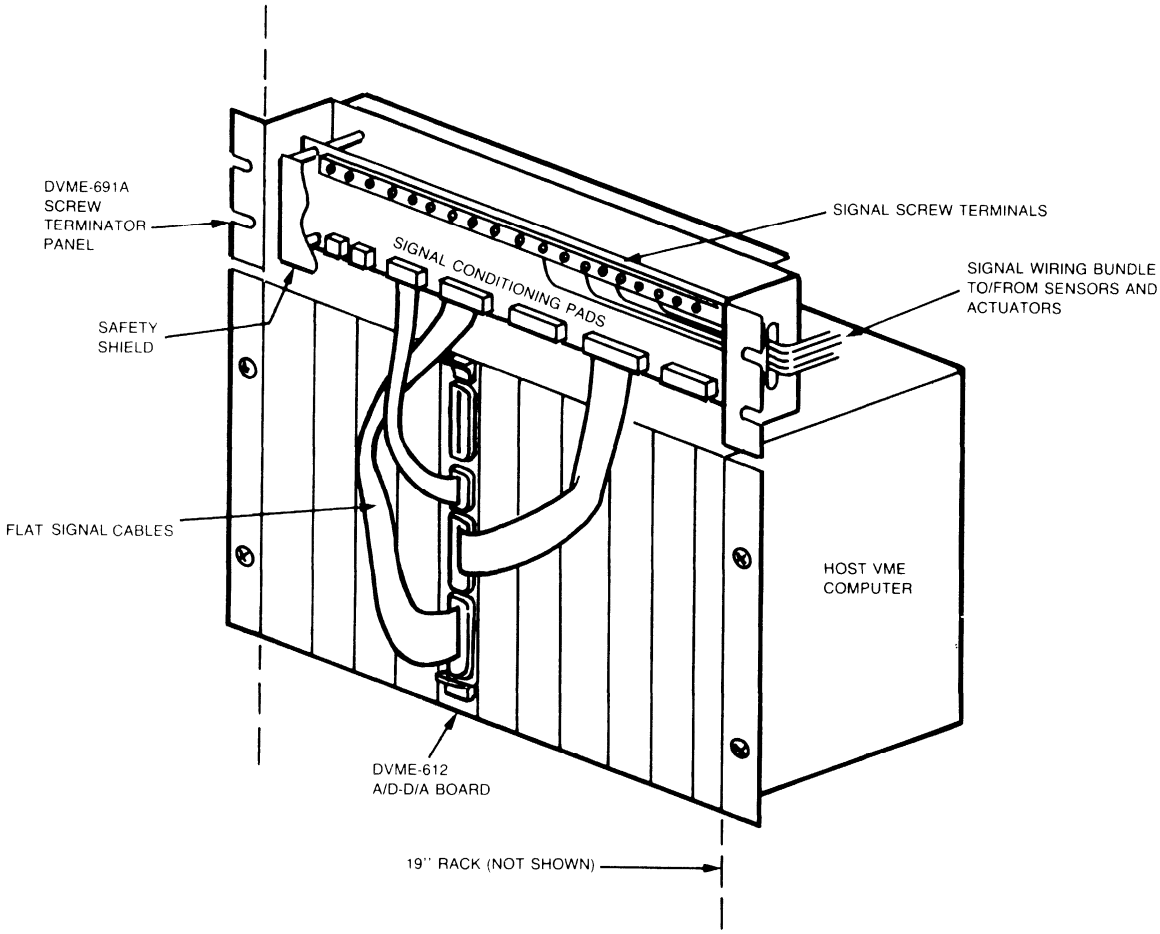


Figure 2. Typical Rack-Mount Configuration

Typical Rack Mount Application
(Figure 2)

This diagram shows the DVME-691 mounted in a 19" rack adjacent to its host computer. Three supplied flat cables connect the DVME-691 to a Model DVME-612 combination A/D-D/A board. The DVME-691 may be positioned either above or below the computer. The cables are each one meter long so that, if required, the 691 may be located in an adjacent rack.

Before connecting the field wiring, the 691's PC board is removed for optional signal conditioning component installation by the user. Signal wiring for input sensors and transducers or output devices connects to the screw terminals along the top of the DVME-691. This wiring may be collected in bundles and routed either through the slots at the ends of the DVME-691 or over the top edge. Wire bundle routing through the slots allows adjacent equipment to be rack-mounted immediately above the DVME-691.

This application uses three flat cables — two for A/D signals and the third for the two DVME-612 D/A channels. User-supplied dc power, if required for sensor excitation or protective clamps, would connect to the screw terminals at the lower left corner of the DVME-691. Ample room is available on the rear mounting bracket to attach a small dc power supply.

Signal Conditioning Pads per Channel
(Figure 3)

This drawing shows the arrangement of PC board circuit pads for each analog channel. The user selects and installs suggested components shown in the illustration. (DATEL will review custom applications under special order). The pad area is intended for a wide range of applications and the user does not have to use the components indicated. As supplied, connections are made straight-through from the screw terminals.

DC power rails are bussed to each channel and are brought out to screw terminals.

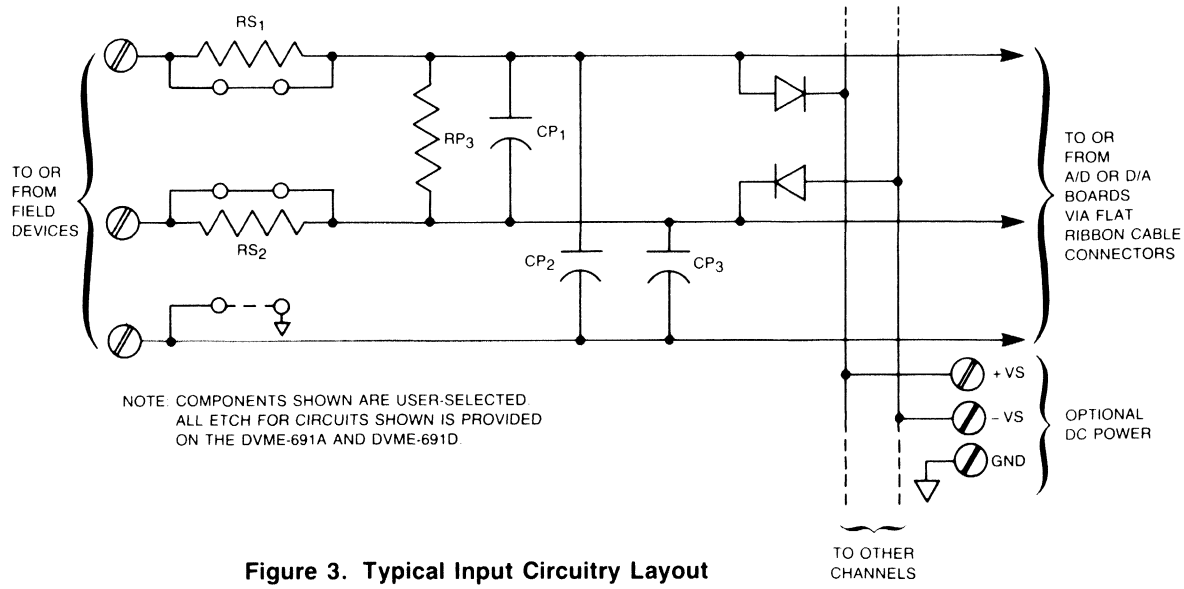


Figure 3. Typical Input Circuitry Layout

Filters and Attenuators

When measuring some signals, it may become necessary to filter out unwanted noise or to attenuate the signals prior to passing them to the analog-to-digital converter board. The DVME-691A provides the user with a convenient area for user-configured passive signal conditioning.

Figures 4, 5, and 6 show typical configurations of simple high-pass, low-pass, and attenuator circuits.

Typical values for a high-pass filter

If the desired cutoff frequency (Fc) is 60 Hz and if Rp is chosen as 10K ohms for differential inputs into the DVME-691,

$$\text{then, } Cs = \frac{1}{2\pi\,(Rp)\,(Fc)} = \frac{1}{2\pi\,(10K)\,(60)} = 0.265\ \mu F$$

Refer to Figure 4, installing a 0.265 μF capacitor in the place of RS1 and a 10K ohm resistor in place of RP3.

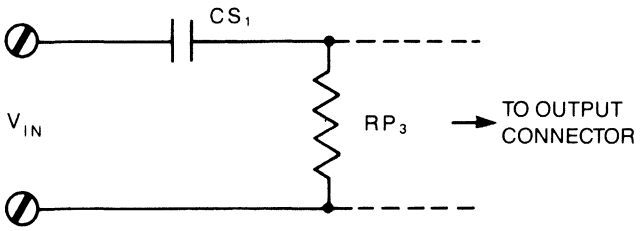


Figure 4. Typical High-Pass Filter

Typical Values For a Low-pass Filter

If the desired cutoff frequency (fc) is 40 Hz, and if Rs is chosen as 20K ohms for single-ended inputs into the DVME-691,

$$\text{then, } Cp = \frac{1}{2\pi\,(Rs)\,(fc)} = \frac{1}{2\pi\,(20K)\,(40)} = 0.2\mu F$$

Refer to Figure 5, installing a 0.2μF capacitor in the place of CP2 and a 20K ohm resistor in place of RS1.

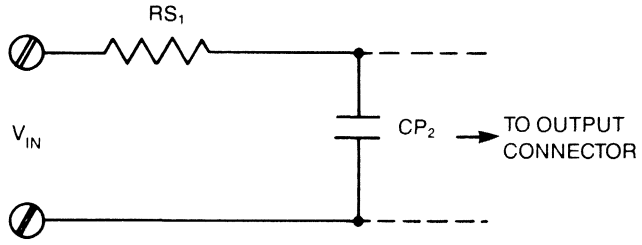


Figure 5. Typical Low-Pass Filter

Typical Attenuator Circuit

If the input signal is 50V dc and the input circuit device can only handle +10V dc maximum, an attenuation circuit can be made up as follows:

If choosing a 100K ohm resistor for Rs,

$$Rp = \frac{Vp\ Rs}{Vin - Vp} = \frac{10(100K)}{50 - 10} = \frac{1\ megohm}{40} = 25K\ ohms$$

Refer to Figure 6, installing a 25K ohm resistor in the place of RS3 and a 100K ohm resistor in place of RS1.

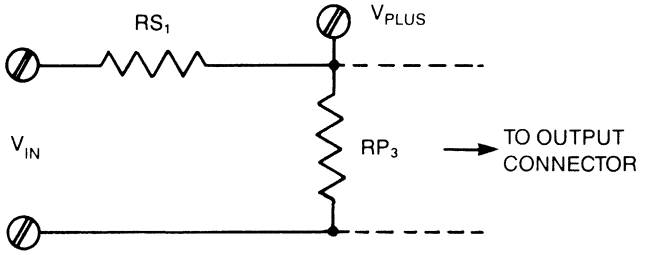


Figure 6. Typical Attenuation Circuitry

ORDERING GUIDE

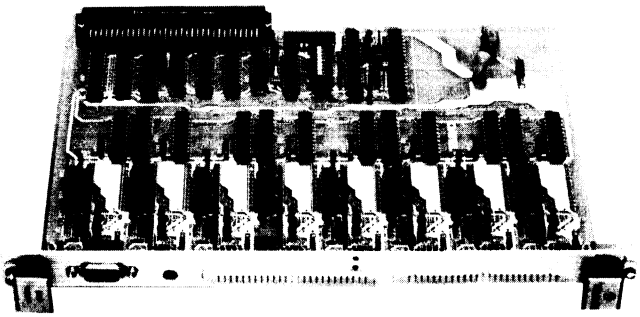
Model Number	Description
DVME-691A (for VME)	Screw terminator panel for 32 single-ended or 16 differential analog input and 2 analog output channels (includes 3 cables for DVME-611/612/601 boards).
DVME-691D (for VME)	Screw terminator panel for 8 analog output channels (includes 2 cables for DVME-62X series boards).

Contact DATEL for custom component configurations.

DVME-660
48-Line Digital I/O VMEbus Board

FEATURES

- **Complete compatibility with VMEbus specifications**
- **48 Digital I/O lines**
- **Software programmable input and outputs**
- **Interrupt levels, IRQ1 through IRQ7**
- **On-board timer**
- **24- and 16-stage timer operation**
- **Interrupts on 1. Timer**
  2. Compare register
  3. External trigger
- **Compatible with GORDOS I/O module systems**
- **Compatible with OPTO-22 I/O module systems**



DATEL EXPANDS ITS VMEbus PRODUCT LINE WITH THE DVME-660. THE DVME-660 HAS 48 INDIVIDUALLY PROGRAMMABLE TTL INPUT OR OUTPUT LINES. THE ON-BOARD HARDWARE INCLUDES AN INTERRUPT CONTROLLER THAT ALLOWS UP TO EIGHT USER-PROGRAMMABLE INTERRUPT LINES AND A TIMER THAT ALLOWS DELAYS UP TO A FEW MINUTES.

GENERAL DESCRIPTION

The DVME-660 is a high-performance digital I/O board that allows programming 48 lines individually. The board is electrically and mechanically compatible with GORDOS and OPTO-22 I/O module systems. The board is ideally suitable for industrial and process control applications.

Functionally the board consists of six bi-directional ports of eight lines each, a programmable timer and a VMEbus interrupter. The data direction of the eight lines in each port is programmable by the host system. The timer may receive the input frequency from the VMEbus SYSCLK signal or an on-board RC network. 16 of 24 timer stages are programmable by the VMEbus data lines. The timer is also programmable to bypass the first eight stages. Figure 1 shows the DVME-660 functional block diagram.

ORDERING INFORMATION

DVME-660

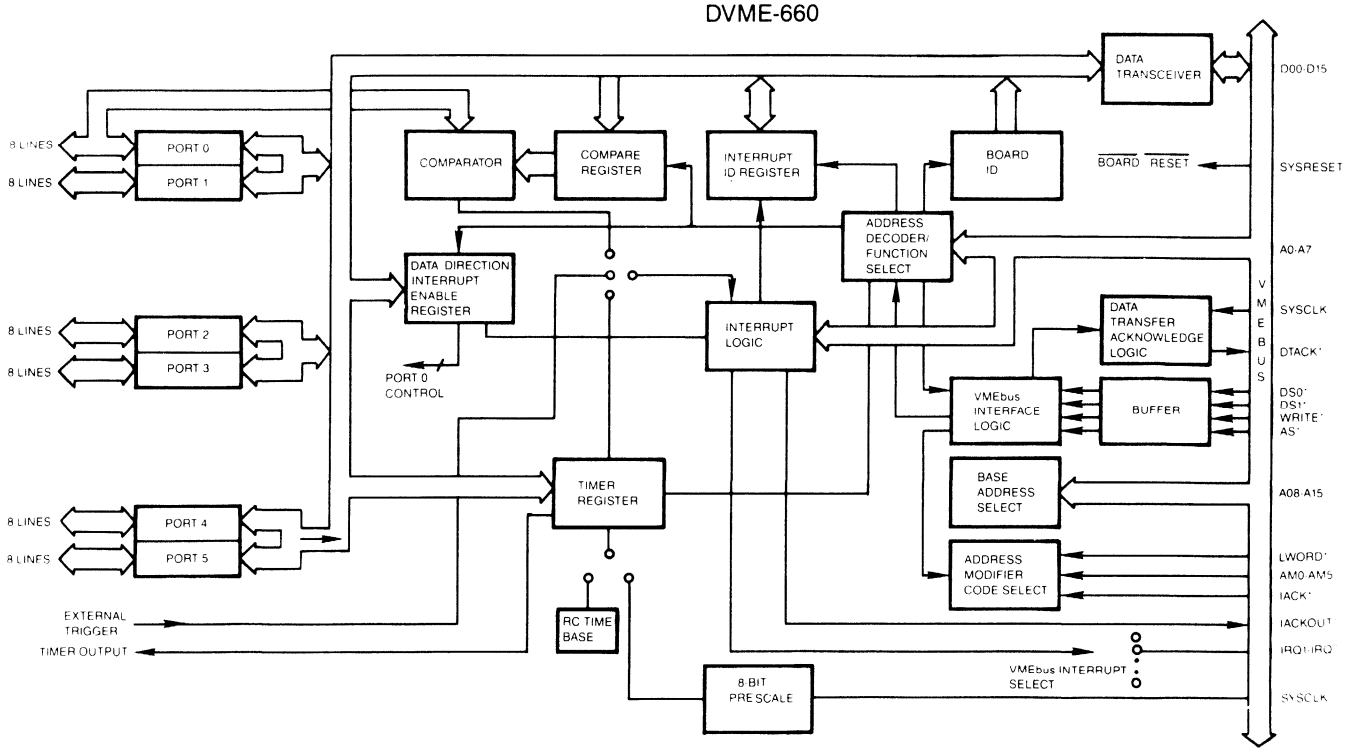


Figure 1: DVME-660 Functional Block Diagram

If enabled, the DVME-660 interrupt logic section generates an interrupt request on one of the VMEbus interrupt lines (IRQ1* through IRQ7*). The interrupt line is jumper-selectable. The interrupt logic accepts a 3-bit interrupt acknowledge level, IACK*, and IACKIN* signals from the host system as interrupt acknowledge and daisy chain input signals. If this interrupt level matches the DVME-660 interrupt request level, the on-board logic loads the interrupt ID number on to the VMEbus. If the level does not match, the board generates the daisy chain IACKOUT* signal. The DVME-660 may generate interrupt request from one of three sources: timer section, port 0 comparator section, or an external trigger. The timer output is jumper-selectable to cause periodic VMEbus interrupts. The board also generates an interrupt if port 0 inputs match data in compare register. The VMEbus data lines (D00 through D07) may load the compare register.

FUNCTIONAL SPECIFICATIONS

(Typical at 25 °C, unless otherwise noted)

INTERFACE SPECIFICATIONS

Data Bus ..... 16 bits (A16:D16 slave)

Address Bus ..... Short I/O space, 16 address lines, 6 address modifier lines. Uses address modifier codes 29H, 2DH, 39H and 3DH

Interrupts ..... IRQ1* through IRQ7*

Memory Mapping ..... Short I/O space, user or supervisor, 256 words allocated per board

Data Transfer ..... DTACK* signal line. Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines. This signal is derived from 16MHz VMEbus clock

I/O SPECIFICATIONS

Number of Port Lines .... 48, programmable as inputs or outputs non-isolated

DIGITAL OUTPUTS

Output Port Current ..... I_{OL} = 24 mA maximum at V_{OL} = 0.5V maximum
I_{OH} = -15 mA maximum at V_{OH} = 2.0V minimum

DIGITAL INPUTS

Input Port Voltage ..... V_{IL} = 0.8V maximum
V_{IH} = 2.0V minimum

Input Port Current ..... I_{IL} = -1.26 mA maximum at V_i = 0.4V
I_{IH} = 20 μA maximum at V_i = 2.7V

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1.3 Amperes, typical ,1.5A max.

VMEbus Interface

The DVME-660 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data input and output purposes. The DVME-660 generates the data acknowledge (DTACK*) signal to notify acceptance of data from the VMEbus data lines, D00 through D15. The DTACK* signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes VMEbus control lines (WRITE*, DS0*, DS1*, and SYSRESET*) to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-660 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector ... 96-pin male connector

Port Connectors J1 and J2 ..... 50-pin header male connectors

Trigger Control Connector J3 ..... 9-pin D-type female connector, DB-95

PHYSICAL CHARACTERISTICS

Outline Dimensions ..... 9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)

Weight ..... 1 lb (453.6 grams)

Operating Temperature Range ... 0 to +60 °C

Storage Temperature Range .... -20 to +80 °C

Relative Humidity ..... 0 to 90%, non-condensing

DVME-660 PROGRAMMING

The DVME-660 maps onto 256 consecutive bytes in the host system's address space. The contents of this address space are the board ID number, data registers, port compare register, data direction/interrupt enable register, interrupt ID register and the programmable timer register. Table 1 lists the contents of the DVME-660 address space.

Table 1: DVME-660 Address Register

Address	Function	Contents
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 64	Read/Write	Data direction/Interrupt enable register
Base + 66	Read/Write	Interrupt ID register
Base + 68	Write	Timer register
Base + 70	Write	Compare register
Base + 72	Read/Write	Port 0 and 1 I/O register
Base + 74	Read/Write	Port 2 and 3 I/O register
Base + 76	Read/Write	Port 4 and 5 I/O register

Data Direction/Interrupt Enable Register

The host system may program bits 0 through 5 of this register to assign direction of the six I/O ports. When programmed, all eight lines in a port will function as either inputs or outputs. Programming the bit 6 of this register enables the on-board interrupt logic. If this bit is set, the DVME-660 interrupts the host system. The interrupt may be from the timer section, the port 0 comparator section, or an external trigger. Figure 2 shows the format of this register.

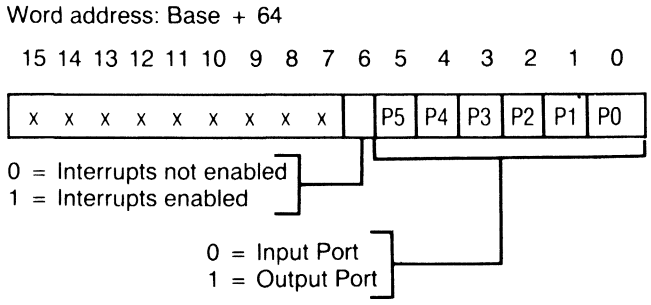


Figure 2: DVME-660 Data Direction/Interrupt Enable Register

Interrupt ID Register

This register contains the user-loaded interrupt ID number. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK* and the daisy chain IACKIN* signal lines. If the DVME-660 interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number onto the VMEbus (low byte). Figure 3 shows the format of the interrupt ID register.

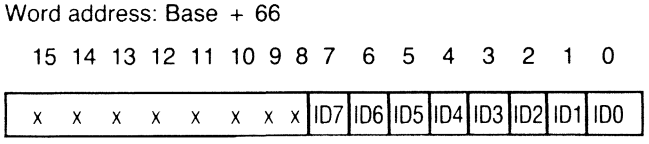


Figure 3: DVME-660 Interrupt ID Register Format

Port Compare Register

The DVME-660 has a port comparator section that compares inputs from port 0 to the contents of the port compare register. The host system may load the port compare register using VMEbus data lines D00 through D07. The port comparator section generates a single VMEbus interrupt if the port 0 inputs match the port compare register contents. Figure 4 shows the format of the port compare register.

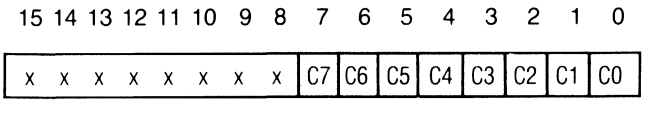


Figure 4: DVME-660 Port Compare Register

Programmable Timer Register

Eight LSB's of this register allows programming the on-board programmable timer section. Bits 0 through 3 assign a timer divide ratio that selects one of sixteen timer stages. The maximum timer input frequency is approximately 1MHz. Bit 4 sets the time for 24 or 16-stage operation by bypassing the first eight stages. Programming bit 6 enables the port 0 comparator. Bit 7 is usable to turn ON an on-board LED lamp. Figure 5 shows the format of this register.

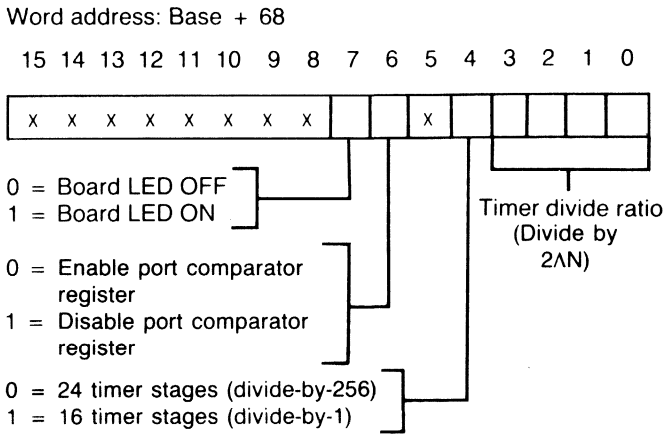


Figure 5: DVME-660 Programmable Timer Register

Port I/O Registers

The DVME-660 uses three 16-bit registers as six 8-line ports. The lower 8 bits of these registers correspond to ports 0, 2, and 4 respectively and the higher 8 bits correspond to ports 1, 3, and 5 respectively. Figure 6 shows the format of these registers.

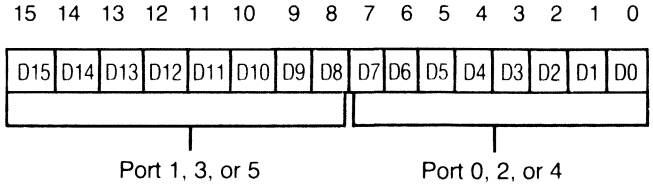


Figure 6: DVME-660 Port I/O Registers

Note: All data is inverted.

I/O CONNECTIONS

The DVME-660 digital I/O board uses J3 connection for trigger control, and J1 and J2 connectors for digital I/O connections. Tables 2 and 3 lists signals for these connectors.

Table 2: Trigger Control Connections (J3)

Pin #	Signal
1	External Interrupt Request In
2	Trigger Output
3	External Timer Clock In
4	No Connection
5,6	+5V dc
7,8,9	Digital Ground

Table 3: DVME-660 I/O Connections (J1 and J2)

J1 Connector		J2 Connector	
Pin #	Signal	Pin #	Signal
47	Channel 0	47	Channel 24
45	Channel 1	45	Channel 25
43	Channel 2	43	Channel 26
41	Channel 3	41	Channel 27
39	Channel 4	39	Channel 28
37	Channel 5	37	Channel 29
35	Channel 6	35	Channel 30
33	Channel 7	33	Channel 31
31	Channel 8	31	Channel 32
29	Channel 9	29	Channel 33
27	Channel 10	27	Channel 34
25	Channel 11	25	Channel 35
23	Channel 12	23	Channel 36
21	Channel 13	21	Channel 37
19	Channel 14	19	Channel 38
17	Channel 15	19	Channel 39
15	Channel 16	15	Channel 40
13	Channel 17	13	Channel 41
11	Channel 18	11	Channel 42
9	Channel 19	9	Channel 43
7	Channel 20	7	Channel 44
5	Channel 21	5	Channel 45
3	Channel 22	3	Channel 46
1	Channel 23	1	Channel 47
49	+5V dc OUT	49	+5V dc OUT
2 through 50	Digital Ground	2 through 50	Digital Ground

DVME-660 Board Identification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	6	
+ 1F	0	

DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

Data Acquisition Boards for Multibus

MULTIBUS I

Model	A/D Channels	A/D Resolution	A/D Speed	PGA	In/Out Ranges	D/A Channels	D/A Resolution	Notes
ST-702	8 D Isolated 1 KV	13 Bits	33 ms	x50, x100	5V Down to 50 mV	None	- -	Direct thermocouple connections, on board linearize and CJC
ST-711 ST-732	32S / 16D	12 Bits	20 µs	x1 to x1 K Software	5V, 10V Down to 50 mV	2 (732)	12 Bits	On board start timer, Interrupt
ST-703	None	- -	- -	- -	2.5V to 10V 4 to 20 mA	4 Isolated	12 Bits	350V Isolation per channel
ST-724	None	- -	- -	- -	5V, 10V 4 to 20 mA	4	12 Bits	
ST-728	None	- -	- -	- -	5V, 10V 4 to 20 mA	4 or 8	12 Bits	
ST-716	None	- -	- -	- -	5V, 10V	4 or 8	16 Bits	
ST-705	8 D	13 Bits	33 ms	x1 to x200	4V Down to 20 mV	None	- -	RS-232 subsystem and CPU, Direct thermocouple connection, linearize, CJC
ST-519	TTL discrete I/O	- -	- -	- -	TTL	- -	- -	72 TTL lines, In/Out, Interrupt

ST-711/732
32 A/D, 2 D/A Channel Analog Boards for Multibus Microcomputers

SPECIAL FEATURES

- **Model ST-711 — 32 Single-Ended, 16 Differential Input A/D Channels**
- **Model ST-732 — 32 Single-Ended, 16 Differential Input A/D Channels plus 2 D/A Output Channels**

COMMON FEATURES

- **Operate with all MULTIBUS compatible microcomputers using 16-, 20-, or 24-bit addressing, 8-bit data transfer**
- **Work directly from RMX-86 Analog I/O Driver operating software**
- **Include a 10-stage jumper-selected, program-gatable pacer start clock, 1 mS to 1 second, crystal-controlled**
- **A/D input accept up to 16 user-installed shunts for 4-20 mA etc., current inputs**
- **FET-Input differential amplifiers accept on-board resistor for fixed high gain up to X1000 (10 mV full scale range)**
- **Include Programmable Gain Amplifier (X1, 2, 4, 8 gains)**
- **Work with the latest 80X86 and 680X0 CPU's**
- **May be used with any language or operating system**

GENERAL DESCRIPTION

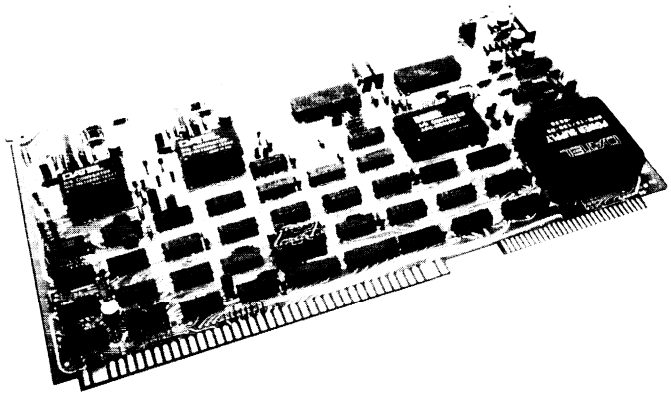
Functionally, DATEL's ST-711 and ST-732 are complete analog input systems for the MULTIBUS iSBC environment. These slide-in peripheral boards accept analog signals from up to 32 single-ended or 16 differential input channels, with the user able to reconfigure the boards using simple jumpers. In addition, the ST-732 provides two digital-to-analog output channels with current loop amplifiers

The differential input channels accept either voltage or current inputs. For current input applications, the user would install shunt resistors across each input channel into circuit pads provided .

Both boards have on-board ±15V power supplies, programmable gain amplifiers (PGA), and a 10-stage crystal pacer clock. Jumpers select the base memory address as well as control the conversion, scan, and external start interrupts.

Other important features include memory-mapped interfacing, addition of a FET input programmable differential amplifier, and complete pin-for-pin form, fit, and function identity to competitive iSBC-711/732 series A/D-D/A board systems. This last feature allows DATEL's ST-711/732 to operate directly from RMX-86 Analog I/O Drivers (Realtime Multitasking Executive Software).

For conversion control, the ST-711 includes on-board registers to store start and final A/D channel address, status bits, conversion modes and interrupt enables.



An A/D Converter auto-increment mode, which is program-selected, automatically advances the channel address after each conversion. Successive A/D samples will continue until the program-selected last channel address is reached.

The ST-732 is identical to the ST-711; both include two 12-bit hybrid DAC-HK D/A converters with input registers.

FUNCTIONAL DESCRIPTION

The A/D sections of the ST-711/732 use DATEL's hybrid technology ADC-HS combined successive approximation A/D converter and Sample/Hold Amplifier. The ADC-HS features 5 microseconds S/H acquisition time and 8 microseconds A/D conversion time and 12 bit binary resolution. System accuracy varies from ±0.05% of FSR ±1/2 LSB (10V range) to ±0.3% FSR ±1/2 LSB (10 mV range), including noise, quantization, nonlinearity, and dynamic errors.

The ST-711/732 employ DATEL's MX-1606 series fast CMOS multiplexers which incorporate ±35 Volts overvoltage protection. Input impedance is 100 meg-ohms minimum (power on) with 30 pA typical input bias current. Balanced inputs require 5 kilohms maximum source impedance to maintain accuracy and throughput rate.

All models inlcude an FET input differential amplifier which is wired as single-ended for the 32-channel models.

The standard A/D-D/A digital coding is offset binary (bipolar) but jumpers may easily be changed to straight binary (unipolar) or 2's complement (bipolar). Standard A/D-D/A analog signal ranges are ±10V full scale but may be jumper selected to ±5V, or +5V, or 10V unipolar.

SPECIFICATIONS

(Typical at 25 °C, dynamic conditions, unless noted).

GENERAL

Configurations available

Model ST-711
32S/16D A/D channels, no D/A channels

Model ST-732
32S/16D A/D channels, 2 D/A channels

Overall System Throughput (high level signals)
23,000 samples/second

ANALOG INPUTS

Number of Channels
32 single-ended or 16 differential
(Jumper-selected. 32S supplied standard)

Channel Expansion
May expand indefinitely by using additional ST-711/732 boards with different base address. Expansion limited by board slots and power.

Input Type
High impedance voltage input, non-isolated. Differential inputs are balanced.

Current Inputs
Up to 16 differential voltage inputs may be converted to differential current inputs with shunt resistors provided and installed by the user. Pads on the board will accommodate 4-20 mA, 1-5 mA, 10-50 mA and other ranges. 4-20 mA ranges require 250Ω, 1/4W ±1% resistors, ±100 ppm/ °C max.

Input Overvoltage
±35V sustained (no damage)

Input Capacitance to Ground
5 pF - Off channels, 100 pF - On channels

Full Scale Input Ranges
±10V, ±5V, ±2.5V, ±1.25V (supplied standard, selectable by 2-bit programmable gain code). Board pads are etched for the user to install a fixed gain resistor, providing down to ±10 mV full scale range.

Programmable Gain Amplifier
Supplied, X1, X2, X4, X8 gains (see ranges above). Fixed high gain X1000 optional (see above)

Input Impedance
100 mΩ minimum, differential or to ground (power on) 1.5 kΩ minimum (power off)

Input Source Resistance for Rated Specifications
5 K Ohms maximum (balanced)
1 K Ohms maximum (unbalanced)

Input Bias Current
30 pA typical, 200 pA maximum

Overall Accuracy at +25 °C
(Including 3-sigma noise and quantization error, dynamic response errors, referred to input, after initial calibration)

Gain	Accuracy
X1	±0.05% FSR ±1/2 LSB
X2	±0.07% FSR ±1/2 LSB
X4	±0.07% FSR ±1/2 LSB
X8	±0.07% FSR ±1/2 LSB
X100*	±0.1% FSR ±1/2 LSB
X1000*	±0.3% FSR ±1/2 LSB

*Requires rewiring diff. ampl. for fixed high gain

Common Mode Voltage Range
Within ±12V of analog common (signal plus common mode)

Common Mode Rejection
At Gain = 1

0 Hz	100 dB
100 Hz	80 dB
1 KHz	60 dB

At Gain = 8

0 Hz	120 dB
100 Hz	100 dB
1 KHz	80 dB

At Gain = 1000 (Requires rewiring dif. amp. for fixed high gain)

60 Hz	100 dB

Nonlinearity
±1/2 LSB

Differential Nonlinearity
±1/2 LSB

Resolution
12 binary bits (1 part in 4096)

Multiplexer Crosstalk from Off Channels
0.01% maximum

Sample/Hold Switch Feed Through
0.01% maximum

Sample/Hold Aperture Delay Time
100 nanoseconds, maximum

System Temperature Coefficients
Gain
±25 ppm of FSR/ °C (Gain X1)
±30 ppm of FSR/ °C (Gain X2, 4, 8)
Zero
±20 µV/ °C

A/D Conversion Period
20 microseconds

Amplifier Settling Time
(Input = ±FSR pk-pk step)
8 microseconds (HL)
110 microseconds (LL)

System Throughput Rate (High Level Inputs)
23,000 samples/seconds

A/D Digital Outputs
Offset binary (bipolar) - Supplied standard
Two's complement (bipolar)
Straight Binary (unipolar)

Output Data Format
12 bit binary group compatible to SBC-Series computers. The A/D Bit 1 (MSB) may be inverted by jumper to 2's complement coding.

ANALOG OUTPUTS (ST-732 only)

Number of Channels
2 non-isolated

Full Scale Output Voltage Ranges

0 to +5V	Jumpers may be rewired
0 to +10V	by the user or by DATEL
-5 to +5V	in OEM quantities
-10 to +10V	(Supplied Standard)

Digital Input coding

Straight binary	Jumpers may be rewired by the user or by DATEL in OEM quantities (Supplied Standard)
2's Complement	
Offset Binary	

Output Impedance
200 milliohms

Output Current
±5 mA, short circuit proof to ground

Slew Rate
10 V/µS (with no Ext. Cap. Load)

Settling Time
4 microseconds to within ±1/2 LSB of final value

Accuracy at +25 °C
±50 ppm of FSR/ °C

CURRENT LOOP OUTPUTS
(Special Quantity order)

Full Scale Current Output Range
4 to 20 mA, unipolar. (May be rewired to other ranges by the user.)
Current Loop Load Resistance
0 to 500 Ohms
Current Loop Voltage Compliance
18 to 30V dc, unipolar, provided by the user
Accuracy at +25 °C
±50 ppm of FSR/ °C

PHYSICAL

Outline Dimensions
12W x 6.75D x 0.5H inches* (305 x 171 x 13 mm)
*Cards may be stacked adjacent if standard 0.60" spacing cages are used.
Pin-for-pin and card guide compatible to the Multibus SBC-Series computers
Weight
22 ounces (0.6 kg)
Operating Temperature Range
0 to +55 °C
Storage Temperature range
-25 to +85 °C
Relative Humidity
10% to 90%, non-condensing
Altitude
0 to 15,000 feet (4600 m)

MISCELLANEOUS

POWER CONSUMPTION
+5V dc ±5% @ 2.5 Amps. maximum
An on-board DC/DC Power Converter operated from +5V, is provided to supply regulated ±15V for linear circuits.
Programming and Architecture Type of Interface
Memory-mapped interface (I/O mapping available)
The ST-711/732 appears to the CPU as 16 consecutive memory locations with 4 unused locations
Compatibility
Pin-for-pin and card guide compatible to the Multibus, SBC-Series computers
Compatible Software
RMX-86 Analog I/O Drivers
Data Transfer - 8 bits only
The board does not make connection to BHEN/
Address Decode
16, 20, or 24 bits

Transfer Acknowledge Delay

The ST-711/732 responds with a Transfer Acknowledge (XACK) with any Read or Write Command. The XACK may be delayed to suit different processors. 16 delay steps are jumper-selected from 50 nanoseconds to 1.5 microseconds. Standard units are set to 50 nanoseconds.

Pacer Clock

Adjustable time-base consisting of a 10-stage binary divider capable of starting A/D conversions in the External Trigger Mode. Time-base periods are jumper-selected and the oscillator may be either crystal or RC controlled. The standard range is 97 microseconds to 1 second.

Interrupts

2 of 3 possible interrupts may be jumper-selected to one or both (INTA and INTB) interrupt lines. The interrupts are EOC (End of Conversion), EOS (End of Scan), and Pacer Clock. They are factory-jumpered as: INTA - EOS, INTB - EOC. Additionally, any of the 8 Multibus interrupts may be wired to any combination of the EOC, EOS Pacer Interrupts.

Memory Base Address

The 16-location starting base address is factory set at 00F700 (hex) but may be reassigned on 16-byte boundaries (LSB = 0) by altering a supplied DIP jumper plug.

Memory Address Assignments (All addresses in hex)

New Addr.	DATEL Supplied	Command	Function
Base + 0	00F700	Write	Load Command Register
Base + 0	00F700	Read	Read Status Register
Base + 1	00F701	Write	Load PGA and Ch. Addr. Register
Base + 1	00F701	Read	Read PGA and Ch. Addr. Register
Base + 2	00F702	Write	Load Last Chan. Addr. Register
Base + 3	00F703	Write	Clear Interrupts
Base + 4	00F704	Read	Read A/D Data LO Byte
Base + 5	00F705	Read	Read A/D Data HI Byte
Base + 8	00F708	Write	DAC 0 LO Byte to Hold Register
Base + 9	00F709	Write	DAC 0 HI Byte
Base + A	00F70A	Write	DAC 1 LO Byte to Hold Register
Base + B	00F70B	Write	DAC 1 HI Byte
Base + C to	00F70C/F &		Don't Use
Base + F	00F706/7		Don't Use

Acknowledge Interrupts (WRITE BASE +3)

Bits	Function
7,6	Not Used
5	0 = Clear EOC Interrupt
4	0 = Clear EOS Interrupt
3	0 = Clear Pacer Clock Interrupt
2,1,0	Not Used

Write to selected bit to acknowledge the interrupt. These bits do not disable interrupts.

A/D CONTROL ADDRESSES

Load Command Register (WRITE BASE + 0)

Bits	Function
7	Not Used
6	Not Used
5	1 = Enable End of Conversion (EOC) Interrupt
4	1 = Enable End of Scan (EOS) Interrupt
3	0 = Clear Board Busy Status
2	1 = Enable External Trigger, 0 = pgm start
1	1 = Enable Automatic Channel Address Increment 0 = Single Channel
0	1 = Enable A/D Conversion

Read Status Register (READ BASE + 0)

Bits	Function
7 (EOC)	1 = A/D Conversion Done, 0 = Data Invalid
6	1 = Scan Done
5	1 = EOC Interrupt Enabled
4	1 = EOS Interrupt Enabled
3	1 = Board is Busy
2	1 = External Trigger Enabled
1	1 = Auto-increment Enabled
0	1 = A/D Conversion Enabled

Read/Load PGA and Start Chan. Address Register (READ/WRITE BASE + 1)

Bits	Function	
7,6	00 = Gain X1 01 = Gain X2 10 = Gain X4 11 = Gain X8	The channel address auto sequences on the EOC rising edge if command 1=1
5	Not Used	
4	$1 = 2^4$	Start Chan. Addr. Select (1 of 32)
3	$1 = 2^3$	
2	$1 = 2^2$	
1	$1 = 2^1$	
0	$1 = 2^0$	

Load A/D Last Channel Address (WRITE BASE + 2)

Bits	Function	
7,6,5	Not Used	
4	$1 = 2^4$	Last Chan. Addr. Select (1 of 32)
3	$1 = 2^3$	
2	$1 = 2^2$	
1	$1 = 2^1$	
0	$1 = 2^0$	

All registers reset to zero at power up.

D/A COMMANDS

Load Hold Register with DAC LO Byte (WRITE BASE + 8 = DAC0, WRITE BASE + A = DAC1)

Bits	Function (Write this byte first)
7	DAC Bit 9
6	DAC Bit 10
5	DAC Bit 11
4	DAC Bit 12 (LSB)
3,2,1,0	Zeros

Load HI Byte to DAC; Load Hold Reg. to DAC (WRITE BASE + 9 = DAC0, WRITE BASE + B = DAC1) Enable DAC Input Register Strobe

Bits	Function* (Write this byte second)
7	DAC Bit 1 (MSB)
6	DAC Bit 2
5	DAC Bit 3
4	DAC Bit 4
3	DAC Bit 5
2	DAC Bit 6
1	DAC Bit 7
0	DAC Bit 8

*A/D-D/A convention is to label the converter's Most Significant Bit as Number 1 (MSB). (Note that D/A addressing is mapped adjacent to A/D addressing.)

A/D DATA ADDRESSES*

Read A/D Data HI Byte (READ BASE + 5)

Bits	Function (Read this byte second)
7	ADC Bit 1 (MSB)
6	ADC Bit 2
'	'
'	'
'	'
0	ADC Bit 8

Read A/D Data LO Byte (READ BASE + 4)

Bits	Function (Read this byte first)
7	ADC Bit 9
6	ADC Bit 10
5	ADC Bit 11
4	ADC Bit 12 (LSB)
3,2,1,0	Not Used, set to zeros

*Read B + 5 starts A/D conversion if command 0 = 1. Allow adequate settling time from channel address change until A/D start. Write 01h to BASE + 0 starts an A/D conversion by software.

The start channel is not reloaded at EOS. The channel address counter continues sequencing unless it is reloaded.

INPUT RANGES

Programmable Gain	Unipolar		Bipolar		Low Level Unipolar	Low Level Bipolar
X1	0 to +5V	0 to +10V	±5V	±10V	Up to +80 mV	Up to ±1V
X2	0 to +2.5V	0 to +5V	±2.5V	±5V	Up to +40 mV	Up to ±500 mV
X4	0 to +1.25V	0 to +2.5V	±1.25V	±2.5V	Up to +20 mV	Up to ±200 mV
X8	0 to +675V	0 to +1.25V	±675V	±1.25V	Up to +10 mV	Up to ±100 mV

(Standard, Offset Binary)

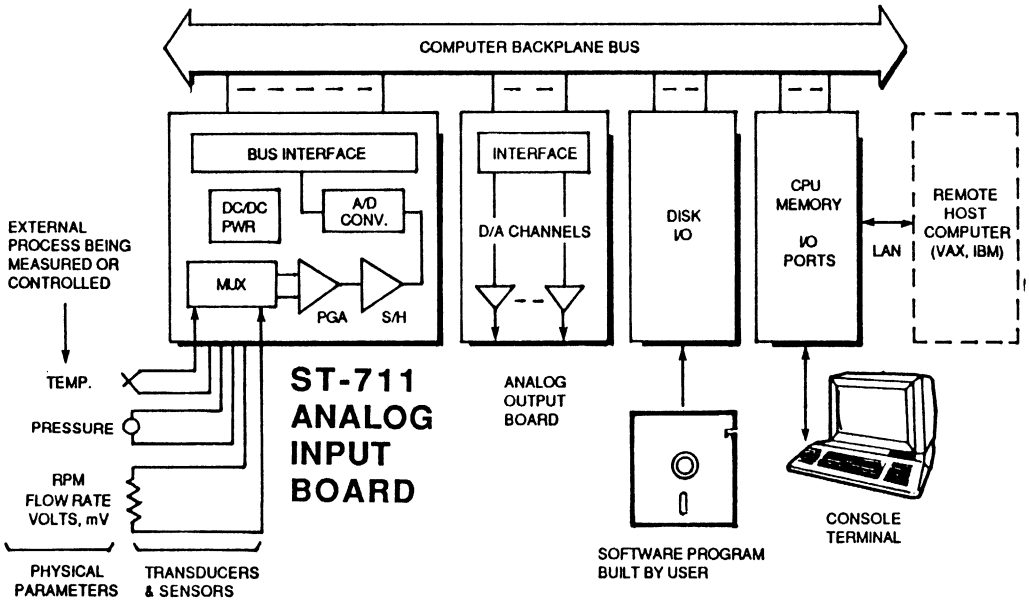
Selected by on-board jumpers

Requires substitution by user of fixed gain resistor on the on-board differential amplifier.

Interface Connectors

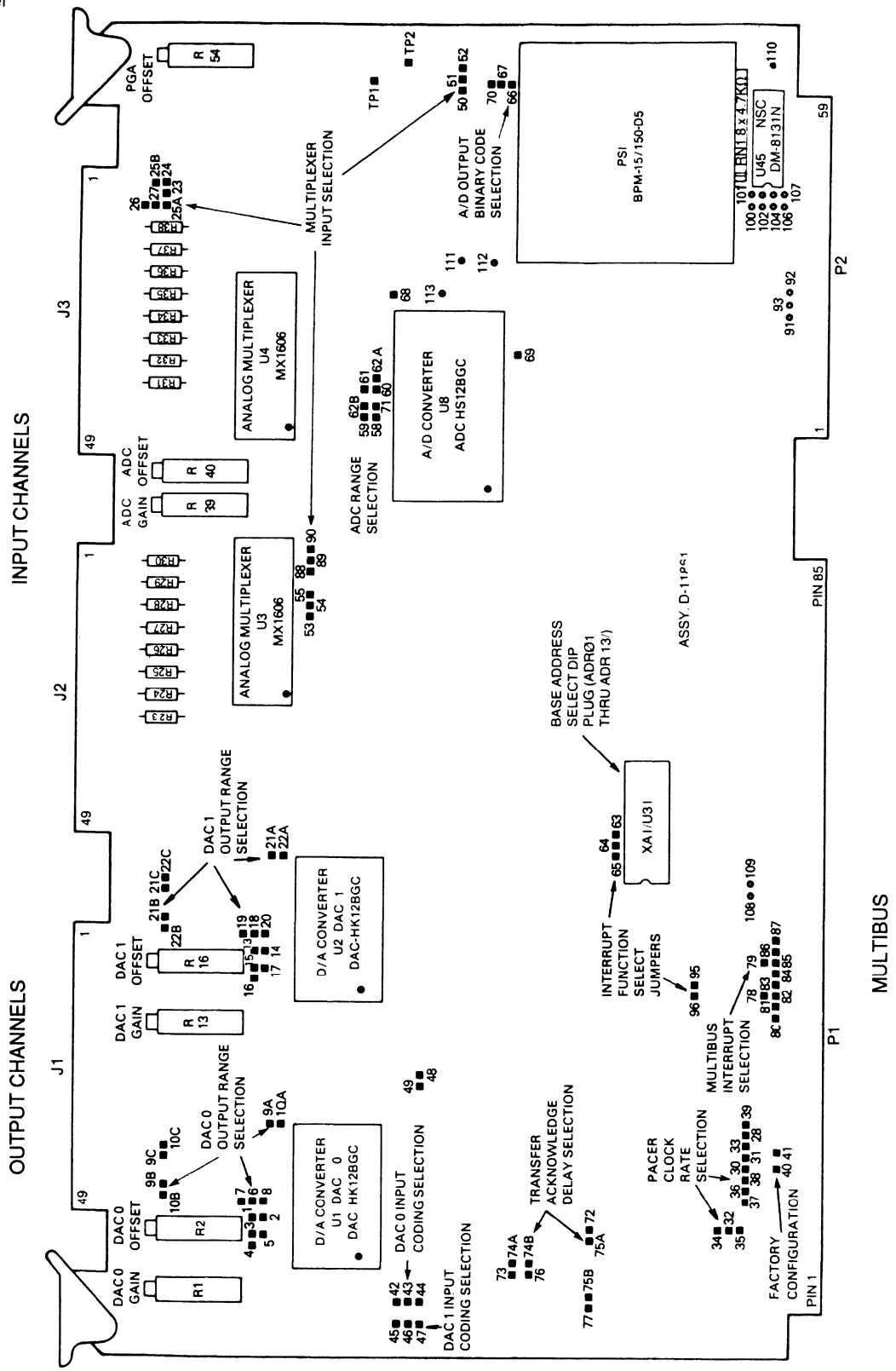
Desig.	Function	No. of Pins	Pin Spacing Centers (in)	Mating Ribbon Connectors
P1	SBC Multibus Bus Connector	86	0.156	–
P2	±15V Aux. Power (Bus)	60	0.1	–
J1	2 D/A Analog Output Channels	50	0.1	58-2076061
J2	1st 8D/16S A/D Input Channels	50	0.1	58-2076061
J3	2nd 8D/16S A/D Input Channels	50	0.1	58-2076061

DATA ACQUISITION COMPUTER



Note: Pin numbering is reversed per Intel convention.

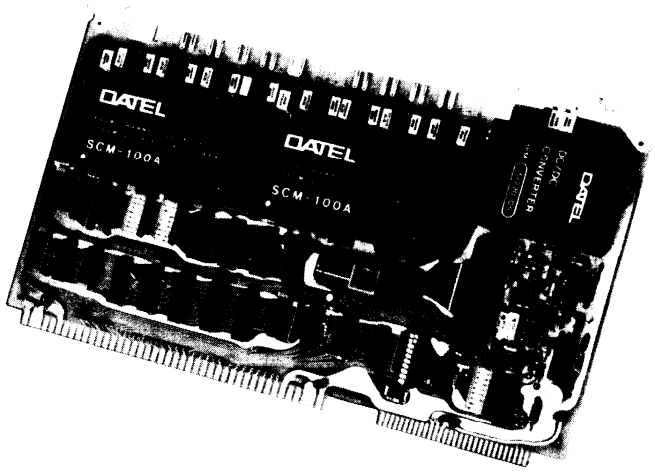
ST-711/732 BOARD LAYOUT



ST-702
MULTIBUS High-Isolation Thermocouple Board

FEATURES:

- **8-Channel MULTIBUS board for temperature measurements**
- **Supports J, K, T, S, B, E, and R type thermocouples**
- **High-level voltage and 4-to-20 mA input capability**
- **On-board CPU for temperature calculation**
- **Up to 1,000V peak input isolation**
- **13-Bit resolution**
- **True electronic cold junction compensation**
- **Output in degrees Celsius or Fahrenheit**
- **128 dB CMRR**
- **55 dB NMR**
- **Screw terminal signal connections**



DATEL's SINETRAC ST-702 is an intelligent MULTIBUS board designed specifically for temperature measurements from J, K, T, S, B, E, and R thermocouples. The 8-channel A/D board filters, amplifies the input signal and provides linearized digital data to a MULTIBUS host system in °C or °F. The board performs as an ideal front-end to programmable controllers and similar systems.

GENERAL DESCRIPTION

The ST-702 is an intelligent MULTIBUS analog input board primarily suited for thermocouple measurements. Features include isolation, 60 Hz line rejection, and screw terminals for input signals. The physical, functional, and electrical attributes of the ST-702 meet and exceed standards demanded by the process control industry.

Low-level isolated analog signals from up to eight thermocouples are filtered, amplified, and converted to digital data using a 12-bit- and sign-integrating A/D converter. The on-board microprocessor linearizes the digital data and outputs a binary quantity directly to the MULTIBUS host computer in degrees Celsius or Farenheit. The ST-702 board also provides electronic cold junction compensation for the thermocouple inputs. The on-board resources relieve the host system of tasks relating to thermocouple linearization.

The ST-702 measures temperature from J, K, S, T, E, R, and B type thermocouples. The analog inputs are galvanically isolated from the MULTIBUS, providing a minimum of 750 Volts RMS common mode isolation. The board's 128 dB Common Mode Rejection Ratio (CMRR) allows thermocouple measurements even in the presence of high common mode voltages. The high isolation protects the host computer from high voltage damages if a thermocouple accidentally contacts a high voltage line. The on-board status register indicates error status information which includes open thermocouple inputs, and over and under range conditions for the thermocouple inputs.

ORDERING INFORMATION

ST-702 ——— Input Type

INPUT TYPE		INPUT RANGES
A	Thermocouple Isolated Types J, K, S, T, E, R, B	J −200 to +760 °C K −200 to +1,232 °C T −200 to +400 °C S 0 to +1,768 °C E −270 to +1,000 °C R 0 to +1,768 °C B +300 to +1,820 °C
		±25.6 mV ±51.2 mV ±102.4 mV
B	High Level Inputs Isolated	±2.500 V ±5.000 V
	Current Loops	0-20 mA 4-20 mA 0-50 mA 10-50 mA

Part No. 60-2105600 Detachable screw terminal analog input connector (formerly No. 60-12474-1).

The ST-702 also measures low level ±51.2 mV or ±102.4 mV full-scale range analog signals from sources other than thermocouples, and provides the raw, unlinearized A/D data to the host CPU. The ST-702 offers gain settings of 1 and 2 when used with low-level voltage inputs.

Applications with high-level signal inputs may use model ST-702B. This model provides ±5V, ±2.5V and current loop signal input capability. High voltage isolation, 1,000V peak, offered by the ST-702 makes it ideal for most industrial applications.

Functionally, temperature is determined by measuring the potential difference between the measurement (hot) junction and the reference (cold) junction of the thermocouple leads. The on-board electronic cold junction compensation logic eliminates errors caused by temperature variations of the cold junction. The CJC is effective over a range of 0 to +60 degrees Celsius.

The ST-702 hardware consists of five sections: MULTIBUS interface section, microprocessor control section, A/D converter section, input signal conditioning section, and CJC section. Figure 1 shows the functional block diagram of the board identifying these sections.

The ST-702 operates from a MULTIBUS host with up to 24-bit addressing capability. The board also supports 8- or 16-bit data transfers, allowing use with 8- or 16-bit MULTIBUS systems. The ST-702 maps onto four consecutive locations in the host system's memory space. Optionally, the board is configurable in the host system's I/O address space using jumper selections. The ST-702's MULTIBUS interface signal includes an XACK/ signal that allows delays from 100 to 800 nanoseconds.

The ST-702 is fully bus and card cage compatible with the MULTIBUS. The board is 12.0 inches wide x 6.75 inches deep x 0.5 inches high (305 x 172 x 13 mm). Multiple ST-702's fit into adjacent card slots of a standard .60 inch spacing card cage. The ST-702 uses power from the MULTIBUS +5V line. The on-board dc-to-dc converter provides ±15V to drive the board's analog circuitry. Total current drawn from the MULTIBUS +5V line is 1.6 A, typical.

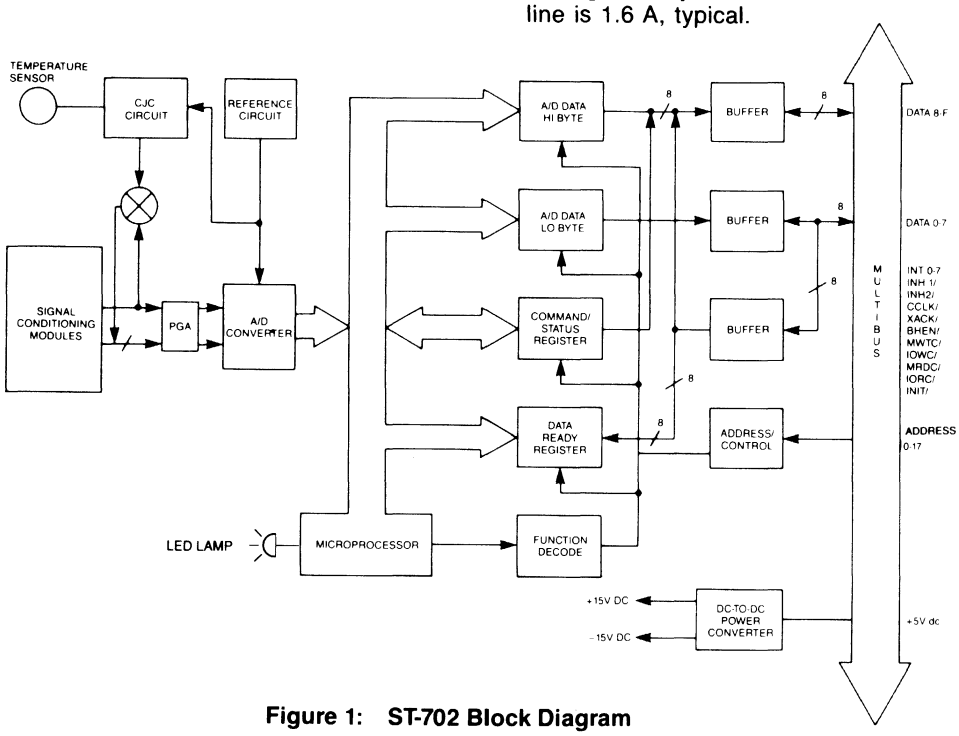


Figure 1: ST-702 Block Diagram

FUNCTIONAL SPECIFICATIONS

All specifications typical at +25 degrees Celsius unless otherwise noted.

Electrical Characteristics

Analog Inputs 8

Input Impedance ..... 100 Megohms

Input Bias Current, maximum ..... 8 nanoamps

Common Mode Voltage Range, Channel to Channel and Channel to MULTIBUS ground AC, 50 or 60 Hz ..... 750V RMS

AC or dc Isolation, peak maximum ..... ±1,000V

Common Mode Rejection Ratio, minimum, Rs = 1k f = 0.01 to 100 Hz
ST-702A ..... 128 dB
ST-702B ..... 110 dB

Maximum Safe Differential Voltage without Damage ..... 130V RMS

Normal Mode Rejection at 50 or 60 Hz minimum ... 55 dB

Input Lead Resistance Effects ..... none

Input Voltage Ranges ..... ±25.6m V
(combined range jumpers and software PGA) ±51.2m V
±102.4m V :702A
±2.5, ±5V dc :702B

Voltage Range Accuracy, maximum
ST-702A ..... 0.03% FSR
ST-702B ..... 0.1% FSR

Voltage Range Gain Drift, maximum ..... 45 ppm/°C

Voltage Range Input Offset Drift

Input Range	Offset Drift (RT I)
±25 mV	3μV/°C
±50 mV	3μV/°C
±100 mV	3.5μV/°C
±2.5 V	55μV/°C
±5 V	55μV/°C

Address bus ..... 16, 20 or 24 bits
Data transfer ..... 8 or 16 bits
using BHEN/, memory mapped (standard) or I/O mapped (jumperable)

Power Supply Requirements

With internal dc-to-dc Converter . . . . . +5V dc ±0.5% @1.6 A

No dc-to-dc Converter . . . . . +5V dc ±0.5% @1.0 A
+15V dc ±0.5% @.15 A
−15V dc ±0.5% @.075 A

Interrupt to MULTIBUS jumperable INT0/ to INT7/ . . . . . 1 line

THERMOCOUPLE INPUT RANGES

Thermocouple Type	Temperature Range (degrees C)	Input Voltage Range (mV)
J	−200 to 760	−7.890 to +42.922
K	−200 to 1232	−5.891 to +49.988
S	0 to 1768	0.000 to +18.698
T	−200 to 400	−5.603 to +20.869
E	−270 to 1000	−9.835 to +76.358
R	0 to 1768	0.000 to +21.108
B	300 to 1820	+0.431 to +13.814

THERMOCOUPLE TEMPERATURE ACCURACY (Maximum) with board at +25°C

Thermocouple Type	Temperature Range (degrees C)	Input Voltage Range (mV)	Accuracy (degrees C)
J	−200 to −100	−7.890 to −4.632	±3
	−100 to +760	−4.632 to +42.922	±1
K	−200 to −100	−5.891 to −3.553	±3
	−100 to +1,232	−3.553 to +49.988	±1
S	0 to +300	0.0000 to +2.323	±6
	+300 to +1,768	+2.323 to +18.698	±3
T	−200 to 0	−5.603 to 0.000	±3
	0 to +400	0.000 to +20.869	±1
E	−270 to −200	−9.835 to −8.824	±10
	−200 to 0	−8.824 to 0.000	±3
	0 to +1,000	0.000 to +76.358	±1
R	0 to +300	0.000 to +2.400	±4
	+300 to +1,768	+2.400 to +21.108	±2
B	+300 to +500	+0.431 to +1.241	±5
	+500 to +1,000	+1.241 to +4.833	±3
	+1,000 to +1,820	+4.833 to +13.814	±2

TIME AND TEMPERATURE RELATED DRIFT

Thermocouple Type	Time related drift (degrees C/6 months)	Temperature related drift (degrees C/degree C)
J	±0.2	±0.1
K	±0.25	±0.15
S	±1.0	±0.3
T	±0.25	±0.1
E	±0.2	±0.15
R	±0.8	±0.3
B	±1.0	±0.3

PHYSICAL/ENVIRONMENTAL

Outline Dimensions . . . . . 12.0 inches wide x 6.75 inches deep x 0.5 inch high (305 x 172 x 13 mm)

Weight . . . . . 1 pound 2 ounces

Operating Temperature Range . . . . 0 to 60 degrees Celsius

Storage Temperature Range . . . . . −20 to +80 degrees Celsius

Relative Humidity noncondensing . . . . . 0 to 80%

Altitude . . . . . 0 to 10,000 feet

ST-702 PROGRAMMING INFORMATION

Programming the ST-702 essentially consists of using four registers. The registers are the Data Ready register, Command register, Status register and the A/D data register. These registers appear as four consecutive locations in the CPU's address space. Table 1 lists the functions of these registers.

Table 1: ST-702 Register Assignments

Address	Function	Register Name	Description
BASE + 0	READ	Data Ready	Read Data Ready status
BASE + 1	WRITE	Command	Write Analog Data command
BASE + 1	READ	Status	Read Analog Data status
BASE + 2	WRITE	—	—
BASE + 2	READ	A/D Data (low)	Read Analog Data, low byte
BASE + 3	WRITE	—	—
BASE + 3	READ	A/D Data (high)	Read Analog Data, high byte

Data Ready Register

The host CPU reads this register to determine if valid data and status information is available in the A/D Data and Status registers. The Data Ready register indicates to the host system if the Command register is ready to receive a new command. Bit 0 is set to 1 when a command is written to the register, then resets to a zero as soon as the command is accepted. Figure 2 shows the format of the data ready register.

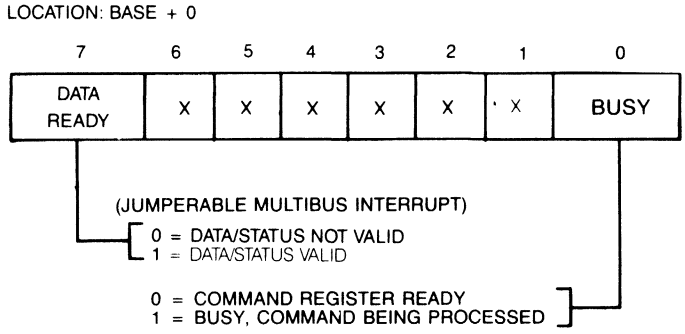


Figure 2: ST-702 Data Ready Register

Command Register

The Command register allows the ST-702 to operate in random mode or sequential mode. Programming the Command register selects the output data coding, PGA gain code, and calibration. The Data Ready register monitors successful completion of the command. Figure 3 shows the Command register format.

LOCATION: BASE + 1

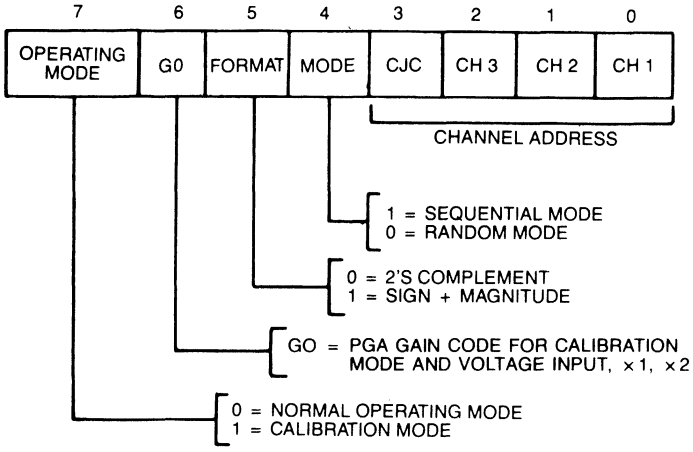


Figure 3: ST-702 Command Register Format

Status Register

The contents of the status register indicate error conditions, channel selected, and the unit for temperature measurement. Figure 4 shows the status register format. The status register determines validity of data in the A/D data register. Bits 4 through 7 of this register indicate open inputs, CJC and data out of range status, and possible ST-702 hardware failures. If the ST-702 fails the self-test at power-up, the status bits indicate RAM or ROM failure and turn the BOARD OK lamp off. If the calibration switch is turned on during normal operation, the status bits indicate this condition. Table 2 lists the error status indications.

LOCATION: BASE + 1

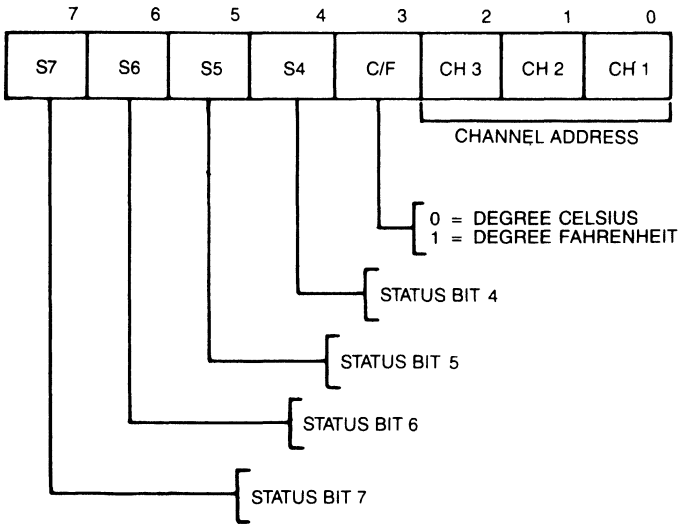


Figure 4: Status Register Format

Table 2: Error Status Conditions

Error Number S7	S6	S5	S4	Error
0	0	0	0	No error
1	0	0	0	Calibration mode
1	0	0	1	Data out of range
1	0	1	0	Open wire detection
1	0	1	1	Board not ready
1	1	0	0	CJC out of range
1	1	0	1	CJC and data out of range
1	1	1	0	CJC or open wire
1	1	1	1	Memory or board failure

A/D Data Register

The A/D data register contains either the raw reading from the A/D converter or the linearized data from a thermocouple, depending on the operating mode. Data is either a 12-bit 2's complement or a sign plus 12-bit number. MSB or sign bit appear in the four MSB positions for ease of sign detection. The data is in a binary format. Figures 5a and 5b show register formats for the A/D data registers.

LOCATION: BASE + 3

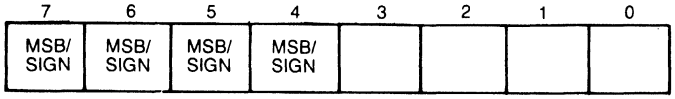


Figure 5a: A/D Data Register Format (High Byte)

LOCATION: BASE + 2

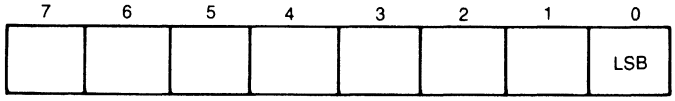


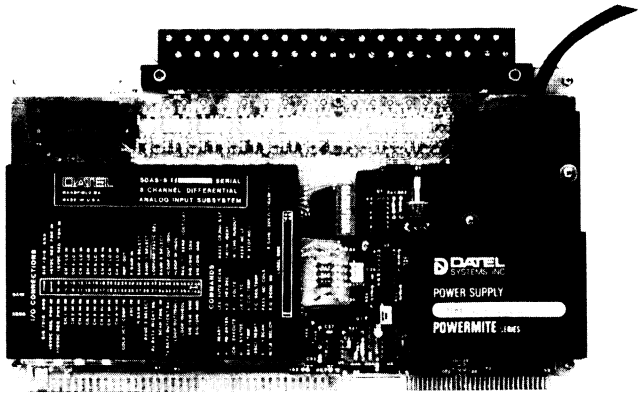
Figure 5b: A/D Data Register Format (Low Byte)

ST-705
Analog Input 8-Channel ASCII Serial Single Board Subsystem

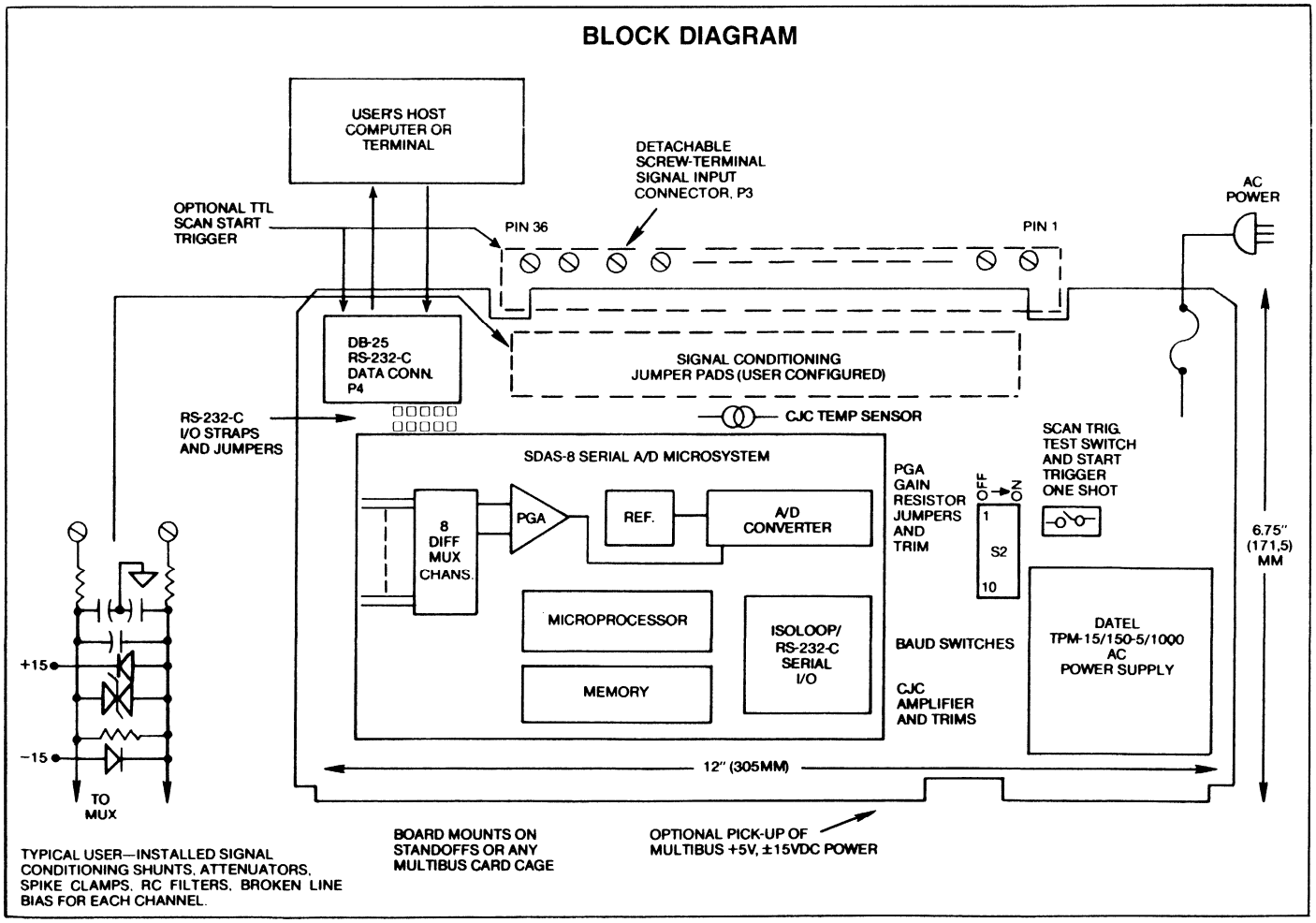
FEATURES

- **8 differential A/D channels using the SDAS-8 microsystem**
- **RS-232-C or 20mA serial isolated loop**
- **Includes input conditioning PC board pads**
- **Includes direct thermocouple measurement with cold-junction temperature sensor and compensation amplifier**
- **Local TTL one-shot scan start trigger from pushbutton or contact closure**
- **Directly connects to Datel's APP-20 and 48 miniature serial thermal panel printers**
- **Selectable gain instrumentation amplifier board pads and trim pot.**

(Refer to the SDAS-8 product literature for full functional description of the SDAS-8 microsystem).



BLOCK DIAGRAM



DESCRIPTION

Designed as a complete, serially accessed 8 channel data acquisition subsystem, the ST-705 is configured on a 12" × 6.75" × 1.7"H MULTIBUS size board.

The ST-705 contains the SDAS-8 data acquisition microsystem, an AC power supply, screw terminal analog input connections and a standard 25-pin RS-232-C DB-25P connector for direct plug-in to the user's terminal or computer. The ST-705 also includes the local thermocouple cold-junction compensation amplifier and connector temperature sensor. For local triggered scan starts, a TTL one-shot circuit accepts an onboard or remotted pushbutton switch or contact closure. Extra PC board pads are included for user-installed input voltage dividers (higher voltage ranges), current shunts (direct 4-20mA measurement, etc.), over-voltage protection clamp diodes or RC hash filters. Barrier screw terminals are installed for an AC line cord.

A board pad matrix is included for user-installed SDAS-8 gain resistors and a gain trim pot is included. These pads would normally be used for the x80 and x160 gain resistors for direct SDAS-8 thermocouple measurement.

The ST-705 may be mounted in a MULTIBUS card cage (available from SCANBE/ZERO, MUPAC, Electronic Solutions, Intel and others) or in the user's host MULTIBUS computer. The ST-705 may also be mounted in a user-supplied separate chassis on standoffs. Although the ST-705 does not connect to MULTIBUS backplane bus signals, pads are included to use +5 Vdc and ±15Vdc power from the host computer, thereby eliminating the ST-705 AC power supply. Using a combination of the transformer-isolated AC supply and the optoisolated 20mA loop serial port, isolation of the analog inputs from the AC line or serial interface is achieved.

USER PC BOARD PADS

There are three primary areas where the user may customize the ST-705 for his application. Caution: This requires mounting and soldering components on a PC board and assumes that the user is skilled at component procurement and electronic assembly. If you need assistance, please contact Datel or a competent engineer.

The three areas are:

1. Input signal conditioning
2. SDAS-8 gain resistor selection and trim
3. Serial port baud rate and pinout strapping

For each of those option areas, refer to the revision level schematic (drawing C-12301) and assembly/layout diagrams (drawing D-12300) for the ST-705 in this brochure.

Input signal conditioning encompasses a wealth of possible options, referring to the schematic drawing. If no conditioning is desired, PC board etch is installed for straight-through unmodified inputs (standard supplied configuration).

The gain resistor pad area includes options for the two fixed thermo-couple gains (J, K require x80; S, T require x160). Also available is a user-selected gain and trim pot pad area.

Serial port board options include baud rate selection using the on-board DIP-switch and RS-232-C handshake pinout options to accept a variety of smart and dumb terminals and host computers. By judicious jumpering, the ST-705 may be made to emulate either an RS-232-C modem DCE device or a terminal DTE device. Most CRT terminals require the ST-705 to interface as a modem. Some small printers and computer serial ports require the ST-705 to interface as a terminal. Many RS-232-C devices ignore the DTR, DSR, CTS, RTS and carrier detect handshakes whereas some require that they are asserted. Refer to the EIA RS-232-C specification and the user documentation of the host device you are connecting to.

The 20mA serial isoloop is normally disconnected from the DB-25P receptacle since no standard 20mA connection exists. Jumpers may be installed as suggested on the ST-705 diagram or at the user's discretion.

The screw-terminal input connector is Datel model 60-12474-1.

MODEL NUMBER/ORDERING GUIDE

ST-705 ___ ___

AC POWER

A = 115 VAC, 60 Hz NMR
E = 230 VAC 50 Hz NMR
J = 100 VAC, 60 Hz NMR
X = AC POWER SUPPLY OMITTED (Requires regulated +5, +/−15 VDC power. May be jumpered from MULTIBUS if available)

(All models accept 47 to 440 Hz. However maximum rejection of AC noise occurs at the normal mode rejection frequencies listed above)

STATION NUMBER

1 = CHANNELS 1-8 (MASTER, ECHOS ALL COMMANDS)
2 = SLAVE, CHANNELS 9-16
3 = SLAVE, CHANNELS 17-24
4 = SLAVE, CHANNELS 25-32

(Use Stations 2, 3, 4 only in 20mA multidrop with Station 1 Master)

Example:
ST-705A1
(115VAC, 60Hz NMR, Master Station 1, Channels 1-8).
A screw-terminal analog input connector is included.

ACCESSORIES/ RELATED PRODUCTS

MODEL/ DESCRIPTION

60-2105600
Spare screw terminal. Analog input connector (One is included with ST-705)

58-2079130
DB-25S serial data mating connector, solder tab. (Optional if you do not have an RS-232 cable).

58-2079260
DB-25P solder tab connector (if required at terminal or computer).

APP-20A21
APP-48A2
RS-232-C/20 mA miniature panel-mount thermal printers. Please request brochures.

TABLE OF CONTENTS

SPECIFICATIONS (Typical @ +25°C)

ANALOG INPUTS

Input Configuration
Differential, high-impedance, true balanced non-isolated, voltage input.

Number of Channels
8 differential channels plus 1 single-ended CJC sensor input

Full Scale Input Range
+/− 4.095Vdc (gain=1)

Thermocouple Temperature Ranges
Type J − 165°C to + 760°C
Type K − 165°C to + 1232°C
Type S − 0°C to + 1768°C
Type T − 200°C to + 400°C

Progammable Gain Amplifier
Resistor-selected up to gain = 200 (+/−20mVdc FSR)

A/D Converter
12 binary bits and polarity
(1 part in 8192), 0.02% FSR linearity

Resolution
1 Count = 1 millivolt at GAIN = 1

Common Mode Voltage Range
+/−11Vdc max to analog ground

Common Mode Rejection
70dB min.

Isolation
20mA serial port optoisolation: +/−2500 V pk, 100 megohms. AC power supply transformer isolation: 1500 VAC, min., 100 megohms, 250 pF

Normal Mode Rejection
40dB @ 50Hz (SDAS-8E), 40dB @ 60Hz (SDAS-8A)

Input Impedance
800 kilohms

Temperature Coefficient
+/−20ppm of FSR°C (GAIN = 1)

A/D Sampling Rate
15 Samples/Sec. (SDAS-8A) to RAM buffer (12.5Hz, SDAS-8E)

COMMUNICATIONS

Data Encoding
Upper case ASCII characters per ANSI X 3.4−1977

Baud Rates
75 to 9600 (Except 110)

Mode
Full duplex, asynchronous

Character Format
1 Start, 8 Data, no parity, 1 Stop bit (all popular 10-bit formats). Output data bit 7(8th bit) = 0

Levels
1. RS-232-C subset, non-isolated
2. 20mA loop, optoisolated

Host Buffer Control
XON, XOFF, (Control Q, Control S) Character encoded

RS-232-C Signals
RxD, TxD, Logic Gnd, Prot. Gnd.

Multidrop
Up to 4 stations, 32D chans., isoloop only, 4 wire

Error Detection
4 ASCII/HEX checksum characters, per A/D scan

DATA TYPES

A/D Data
Selectable decimal/hexadecimal

Thermocouple Data
Linearized to J, K, S, T, Fahrenheit/Celsius conversion, cold-junction compensated

Time of Day Clock
23:59:59 hours, 1 second resolution, 0.05% crystal accuracy

Status Message
Hex encoded and text

A/D SCAN TRANSMISSION START

1. Polled by remote serial command
2. Auto-start from internal timer, command-selected 1 second to 17:59:59 hours
3. Local TTL event trigger input or switch closure.

LINK COMMAND TYPES

Line length (20 to 132 characters), editing, clock controls, A/D controls, resets, data select, terminal controls

PHYSICAL

Outline dimensions
6.75" X 12.00" X 1.62" (171,5 X 304,8 X 41,15mm) excluding standoffs,
MULTIBUS format

Operating Temperature
0° to +60°C

Power Required
Choice of:
115 VAC, +/−10%, 60-440Hz
230 VAC, +/−10%, 48-440Hz
100 VAC, +/−10%, 48-440Hz

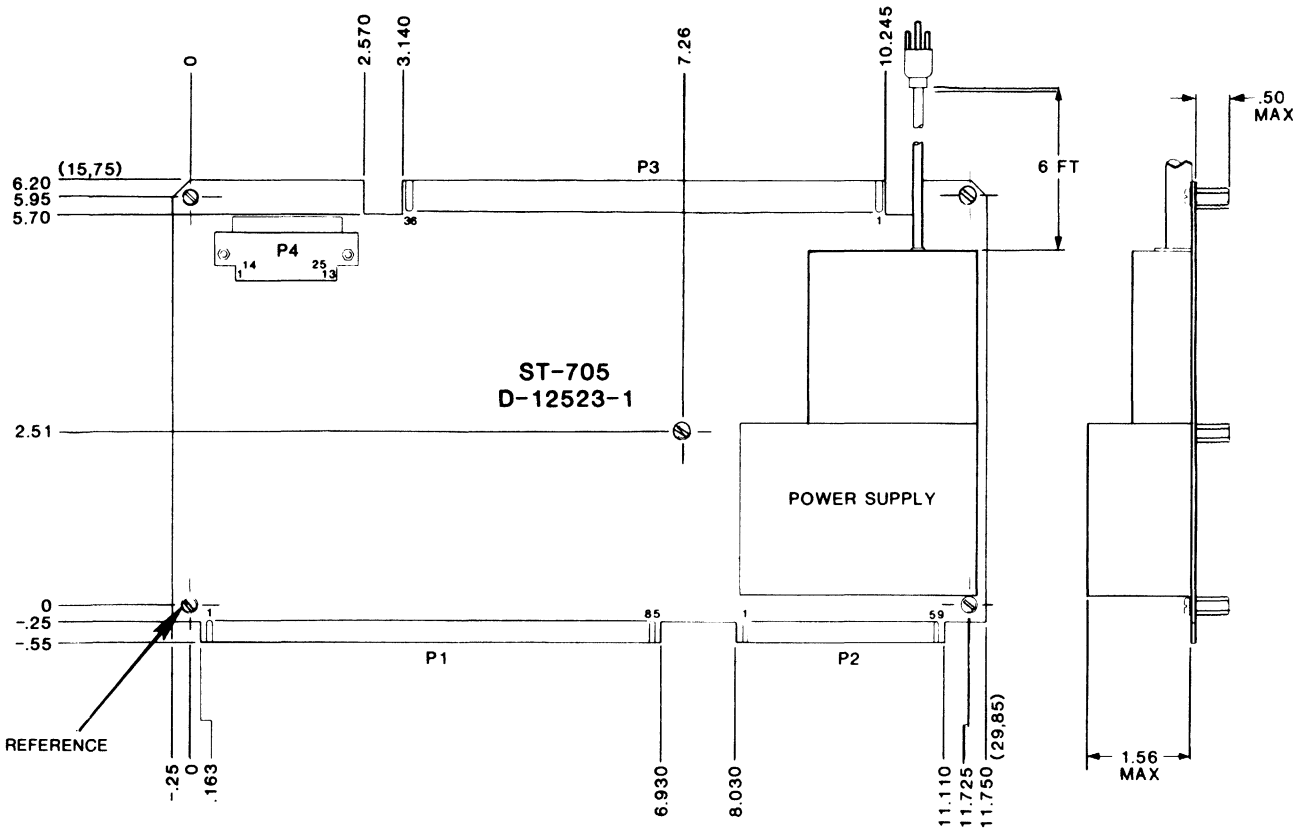
Analog Input Connector
Screw terminal detachable from PCB edge fingers, 0.200" centers, Datel #60-2105600.

Serial Data Connector
DB-25P 25-pin suitable for most RS-232-C devices.

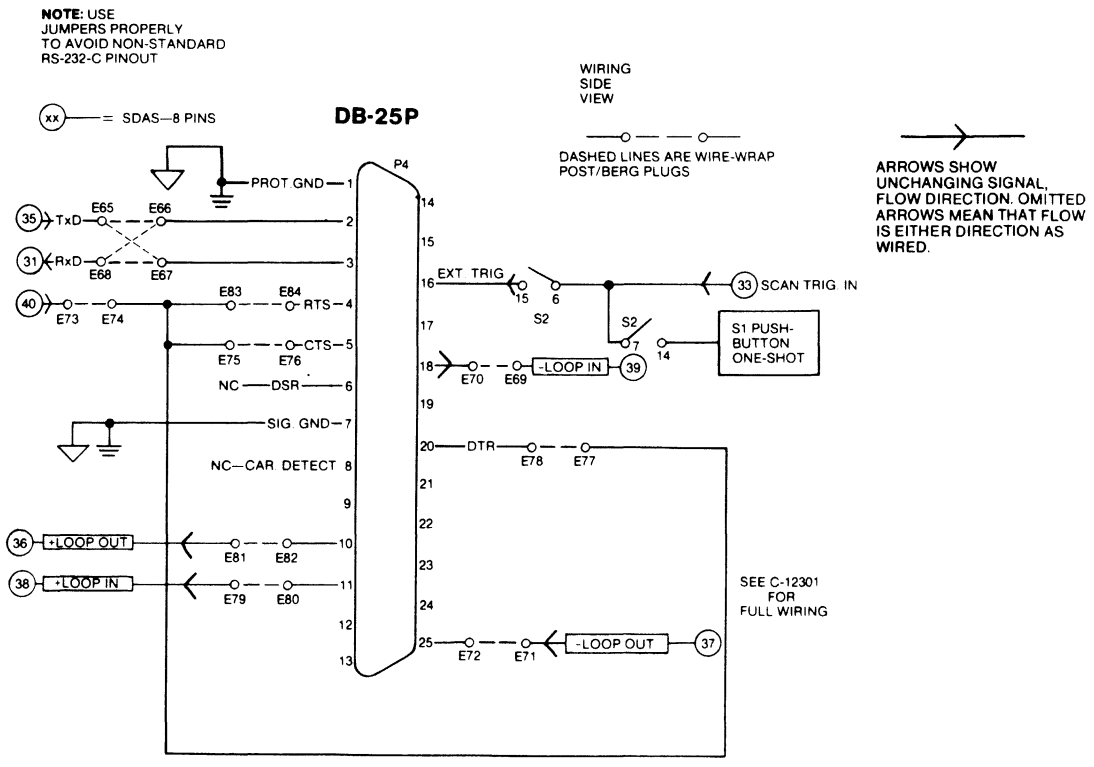
MULTIBUS is an Intel Corp. trademark.

For detailed information about the SDAS-8 Data Acquisition Microsystem mounted on ST-705, refer to the SDAS-8 User's Guide, available on request.

OUTLINE DIMENSIONS
Inches (mm)



P4 DATA CONNECTOR WIRING



RS-232-C SERIAL DATA INTERFACE

The serial data connections shown describe interface to three common RS-232-C devices: most terminals, computer serial ports and modems. There are several basic rules to properly interface to RS-232-C devices. They are:

(1) One end must be the "modem" (DCE device) and the other must be the "terminal" (DTE device). This has to do with the direction of data transmission on pins 2 and 3 of the RS-232-C interface and not the function of the actual devices.

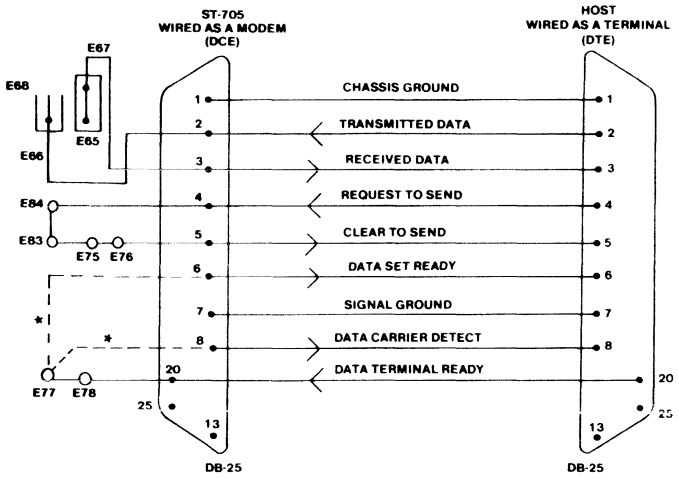
Most modems are wired as DCE devices. Most terminals are DTE devices, as you would expect. Many computer serial ports are DTE but some are DCE. The ST-705 may be jumpered either way. Do not let line names confuse you. Instead, observe the direction of signal flow shown by the arrows in the diagrams.

(2) Most RS-232-C devices require connection to the important handshake signals shown. The ST-705 does not use these handshakes but contains a mini "breakout" function to accommodate correct connection of these handshakes. Minimal RS-232-C connection to ST-705 requires only pins 2, 3 and 7 between AC-isolated devices.

(3) The character coding, length and protocol between both ends must agree. ST-705 ASCII usage is widely accepted for terminals and computers. Modems are transparent to coding conventions.

For further background, consult the EIA RS-232-C specification and other references on data communications.

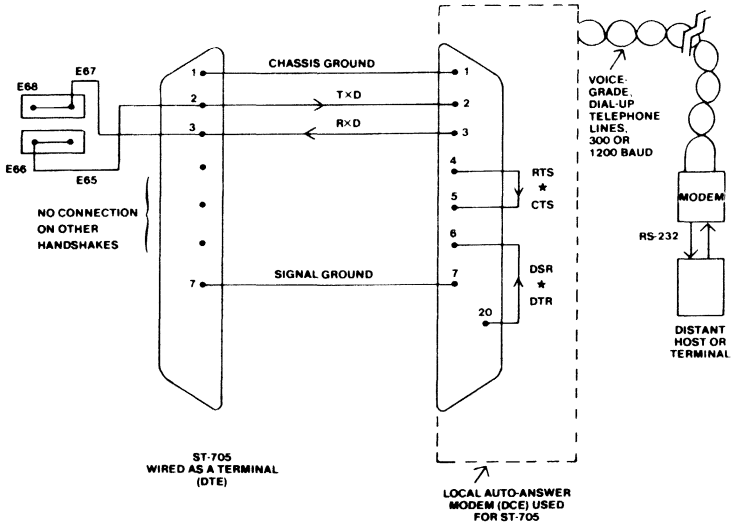
WIRING TO MOST TERMINALS AND COMPUTER SERIAL PORTS



* User-installed optional jumper connections DTR-DSR (pins 20-6) and DTR-DCD (pins 20-8) may be required for many terminals.

The connections shown above will work for most terminals and computer serial RS-232-C ports wired as a terminal. (Consult your computer technical documentation.)

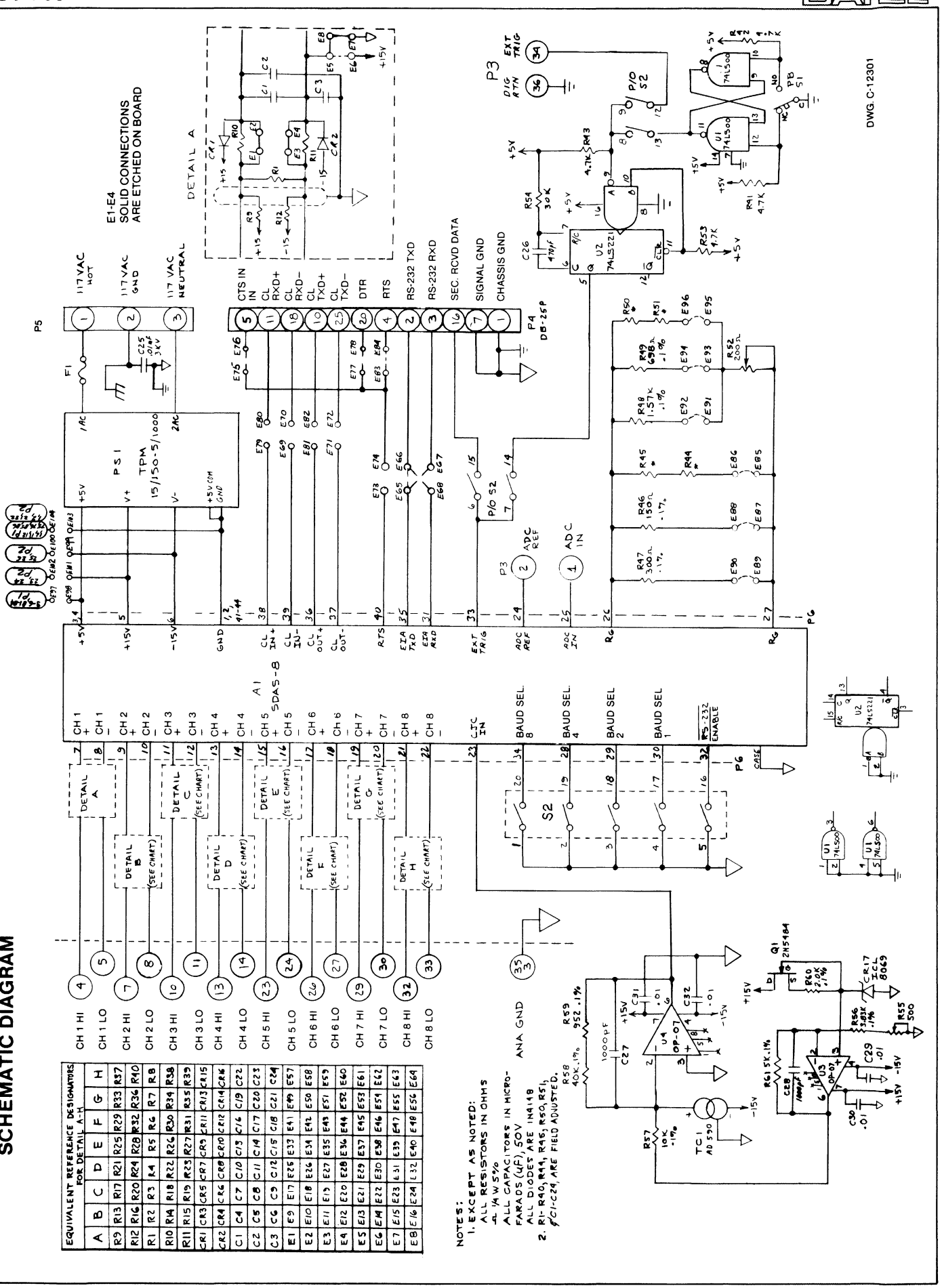
WIRING TO MOST RS-232-C MODEMS



* Many modems require RTS and DTR to be asserted. This may be jumpered as shown on the modem connector or on the ST-705. The ST-705 does not require these handshake signals.

DATEL®

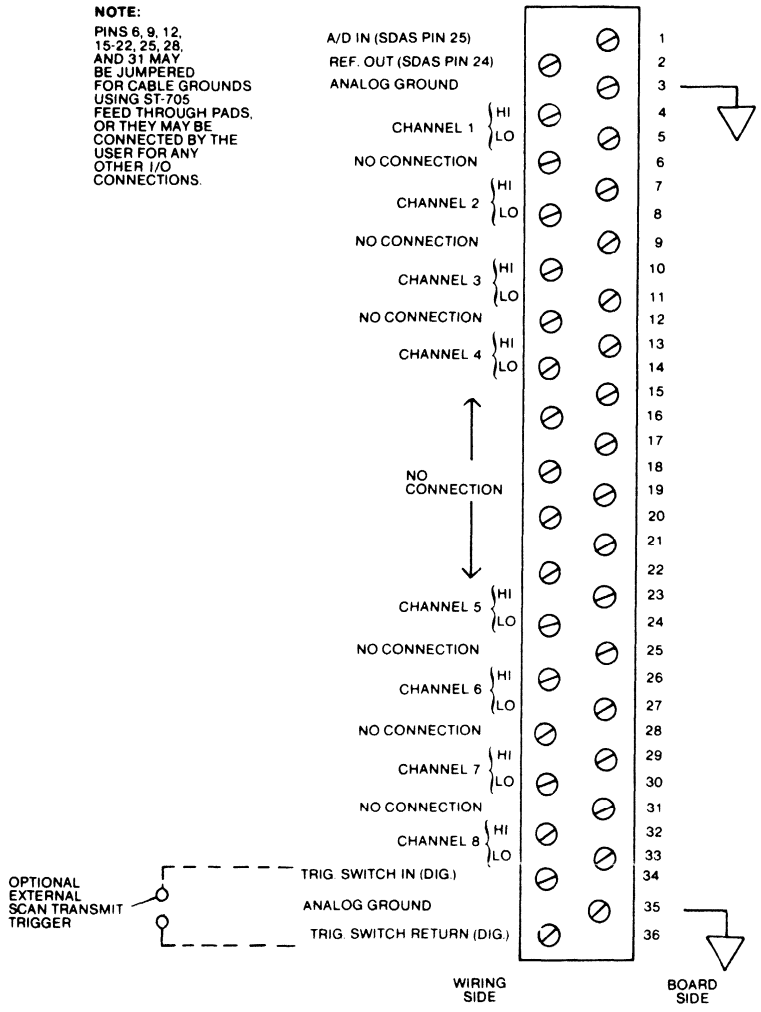
SCHEMATIC DIAGRAM



EQUIVALENT REFERENCE DESIGNATORS FOR DETAIL A-H							
A	B	C	D	E	F	G	H
R9	R13	R17	R21	R25	R29	R33	R37
R12	R16	R20	R24	R28	R32	R36	R10
R1	R2	R3	R4	R5	R6	R7	R8
R10	R14	R18	R22	R26	R30	R34	R38
R11	R15	R19	R23	R27	R31	R35	R39
CR1	CR3	CR5	CR7	CR11	CR13	CR15	
CR2	CR4	CR6	CR8	CR10	CR12	CR14	CR16
C1	C4	C7	C10	C13	C16	C19	C22
C2	C5	C8	C11	C14	C17	C20	C23
C3	C6	C9	C12	C15	C18	C21	C24
E1	E9	E17	E25	E33	E41	E49	E57
E2	E10	E18	E26	E34	E42	E50	E58
E3	E11	E19	E27	E35	E43	E51	E59
E4	E12	E20	E28	E36	E44	E52	E60
E5	E13	E21	E29	E37	E45	E53	E61
E6	E14	E22	E30	E38	E46	E54	E62
E7	E15	E23	E31	E39	E47	E55	E63
E8	E16	E24	E32	E40	E48	E56	E64

NOTES:
1. EXCEPT AS NOTED:
   ALL RESISTORS IN OHMS
   ±1% W 5%
   ALL CAPACITORS IN MICRO-FARADS (μF), 50V
   ALL DIODES ARE IN4148
2. R1-R40, R44, R45, R50, R51, & C1-C24, ARE FIELD ADJUSTED.

DETACHABLE ANALOG SIGNAL INPUT CONNECTOR, P3



POWERING THE ST-705X FROM MULTIBUS

As an alternate mounting method, users may install model ST-705X in a low-cost MULTIBUS card cage. Although no digital connections are made to MULTIBUS, +5V power connections are standard MULTIBUS. Some computers include +/−15Vdc power supplies at the standard P2 locations shown. If preferred, a separate isolated 5 and 15 volt DC supply may be bussed along MULTIBUS to drive one or more ST-705X's in multidrop.

(Caution: This is for the ST-705X only, which omits the AC isolated power supply. Using DC power from a MULTIBUS host may no longer be isolated, causing safety, damage and data error difficulties).

MULTIBUS regulated DC power	Close jumpers	Power supplied through
+5Vdc @ 500mA	E97-E98	P1 pins 3-6, 81-84
+15Vdc @ 50mA	E101-E102	P2 pins 23, 24
−15Vdc @ 50mA	E99-E100	P2 pins 25, 26
Power Return	E103-E104	P1 pins 1, 2, 11, 12 75, 76, 85, 86 P2 pins 1, 2, 21, 22

BAUD RATE SELECTION

SDAS-8 PIN = (34 BAUD 8 SEL.) (28 BAUD 4 SEL.) (29 BAUD 2 SEL.) (30 BAUD 1 SEL.)

BAUD RATE	S2 DIPSWITCH = 1	2	3	4
75	1	0	0	1
150	1	0	0	0
300	0	1	1	1
600	0	1	1	0
1200	0	1	0	1
2400	0	1	0	0
4800	0	0	1	1
9600	0	0	1	0

ON = "0", OFF = "1"

S2 GROUNDS SELECTED PIN

PROGRAMMABLE GAIN AMPLIFIER

Usage	Gain	Jumper	Notes
Type J & K Thermocouples	× 80	Close E89-E90 E91-E92 Only	Trim Full Scale Gain with R52
Type S & T Thermocouples	× 160	Close E-87-E88 E93-E94 Only	Trim Full Scale Gain with R52
User-selected Gain	R Gain = 20KΩ÷ (Gain-1)	Close E85-E86 E95-E96 Only	Install Resistors at R45, R44 with Trims at R50, R51. Choose low resistor Tempco to avoid degrading accuracy.

LOCALLY-TRIGGERED SCAN TRANSMISSION

INPUT TYPE	INPUT CONNECTIONS	DIP SWITCH S2 (Close=ON, Open=OFF)
10 Microsecond positive TTL Pulse	P4: input, pin 16 ground, pin 7	Close S2 SW.6 Open S2 SW.7
Switch closure to ground. (P3, PIN 34 includes a 4.7 Kilohm pullup to +5V)	P3: switch, pin 34 return, pin 36	Open S2 SW.6 Close S2 SW.7 Open S2 SW.8 Close S2 SW.9
ST-705 on-board pushbutton S1	None	Open S2 SW.6 Close S2 SW.7 Close S2 SW.8 Open S2 SW.9

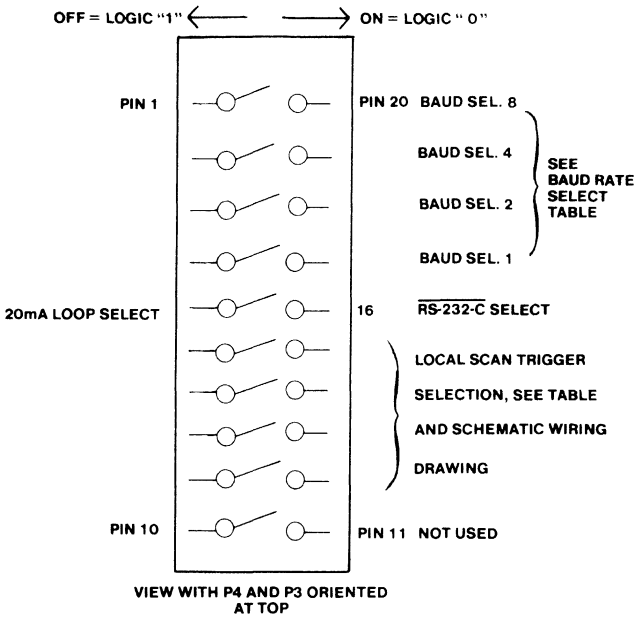
SERIAL CHARACTER FORMATS RECEIVED

START BIT	DATA BITS (LSB first)	PARITY BIT	STOP Bit(s)
1	7	None	2
1	7	Odd, Even, ϕ* or 1	1
1	8	None	1

*Upper case ASCII characters transmitted from ST-705 set data bit 7 equal to logic 0.

ST-705 doesn't care about received character parity.

DIPSWITCH, S2



A/D CODING TABLE

Input Volts (R GAIN = ∞ no connection)	Hexadecimal Display*	Decimal Display
+4.096V	+++++	+++++
+4.095 V	0FFFH	+4.095
+2.048V	0800H	+2.048
+1.024V	0400H	+1.024
+0.256V	0100H	+0.256
+0.002	0010H	+0.002
+0.001	0001H	+0.001
0.000	0000H	+0.000
−0.001	FFFFH	−0.001
−0.002	FFFEH	−0.002
−0.256V	FF00H	−0.256
−1.024V	FC00H	−1.024
−2.048V	F800H	−2.048
−4.095V	F001H	−4.095
−4.096V	-----	-----

*In hex, the polarity bit 12 has been extended to the top 3 MSB's (Bits 13, 14 15)

SERIAL COMMAND SUMMARY

LEGEND:

1. XXX — X are characters entered and displayed on the terminal.
2. ( ) are blind control characters (such as carriage return or escape) which do not appear on the terminal.
3. Carriage return (CR) requests the SDAS-8 to execute the command consisting of the previous character string. Terminate all commands with "Return" or "Enter".
4. The asterisk (*) confirms that the command was executed, and is ready for the next command.
5. The pound sign (#) indicates that the returned character string is not executable. Re-enter a corrected string.

COMMAND EXAMPLES

* — Power-up prompt. Previous command executed; ready for next command
# — Echoed string not executable; try again
G(CR) — Display status message
B(CR) — Display time (HR:MIN:SEC)
B23:59:59(CR) — Set time in 24 hour format
(Escape) — Reset all controls to power-up status except clock
(DEL or backspace) — Delete previous character for editing before execution
(Control S or DC3 or XOFF) — [13HEX] Stop transmission immediate and wait
(Control Q or DC1 or XON) — [11HEX] Start transmission immediate, mid string
R — Stop output transmission from SDAS-8. Stop L mode auto-start timer. (CR) not required. Revert to trigger or polled-start mode.

A/D CONTROLS

X(CR) — Display one scan
M:2(CR) — Set up to display channel 2 only
M:1,8(CR) — Set up to display channels 1-8
L02(CR) — Start automatic scan transmissions every 2 seconds. R or (ESC) are the only way to stop L mode.
L59:59(CR) — Start automatic scan transmissions every 59 minutes: 59 seconds
L17:59:59(CR) — Start automatic scan transmissions every 17:59:59 hours:minutes/seconds (max.)
H(CR) — Format A/D data as hexadecimal ASCII
D(CR) — Format A/D data as decimal ASCII (cancel hex)
V(CR) — Format A/D data as DC volts, (cancel thermocouple)
J(CR) — Format A/D data linearized to selected thermocouple
K(CR)
S(CR)
T(CR)
A(CR) — Transmit A/D data from CJC channel, equivalent ambient temperature. Range +/−99°C.
F(CR) — Format A/D data as Fahrenheit
C(CR) — Format A/D data as Celsius

TERMINAL CONTROLS

W(CR) — Toggles between rubout echo as BS-SP-BS or /X where X is the last character
P80(CR) — Set column width to 20, 40, 48, 72, 80 or 132 (20 = power up state)
E(CR) — Echo all printables (power up state) for full duplex
Q(CR) — Don't echo printables (for half duplex)
Nnnn(CR) — Insert nnn nulls between, CR, NULL's, LF, (Range ϕ -254)
N255(CR) — Suppress line feed. End all scans with CR, (NULL's), no line feed. N255 (CR) is a toggle, which cycles on and off with each application. Confirm the line feed status bit using the G status.
I:nnn - n(CR) — Start all A/D scans with the Ident character string nnn - n (20 characters max)
Cancel with I:(CR)
All lower case printables - Echo if selected. Not acted upon.
All non-specified controls - Echo if selected. Not acted upon.
BN(CR) — Delete time and station
BY(CR) — Resume time and station

POWER UP MODE

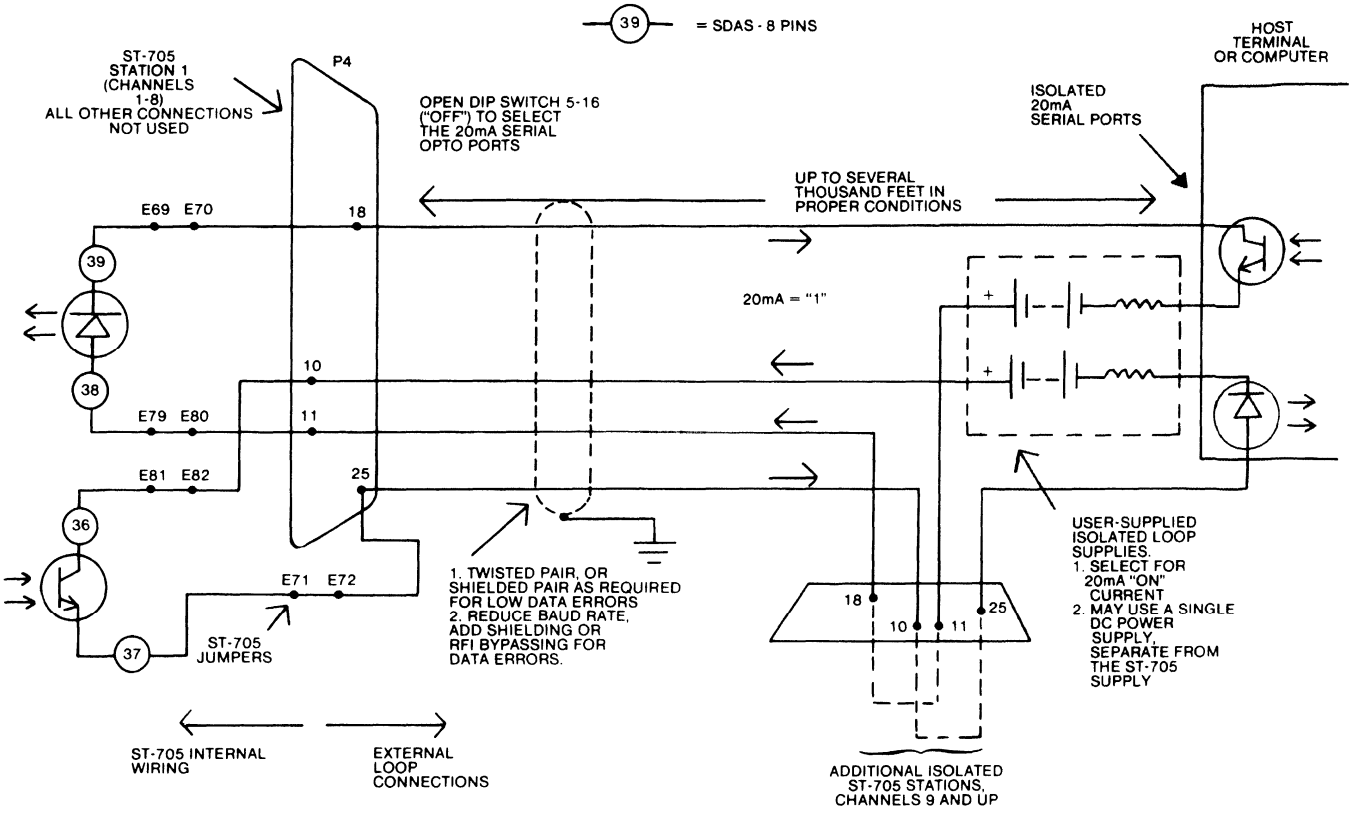
Station 1
20 characters per line
Trigger/polled scan start
8 channels, 1-8
Echo on

Elapsed time from power-on
The line terminator sequence at power up is:
<CR, NUL, NUL, - (216 NUL's), no LF>

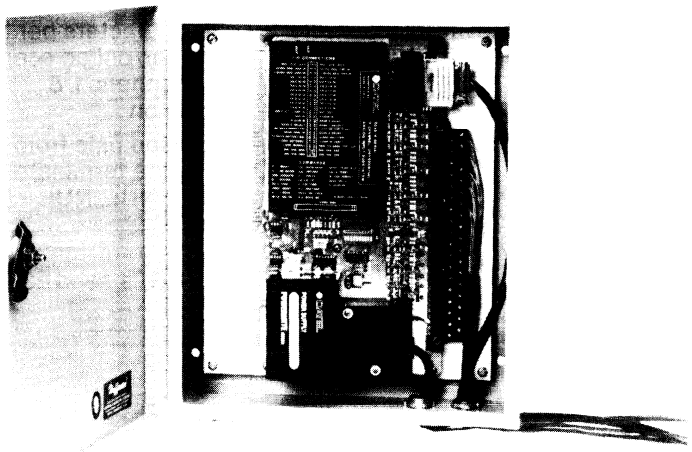
VERY IMPORTANT

For CRT's, send ESCAPE first to cancel the NUL's and restore LF.

TYPICAL 20mA ISOLOOP MULTIDROP WIRING



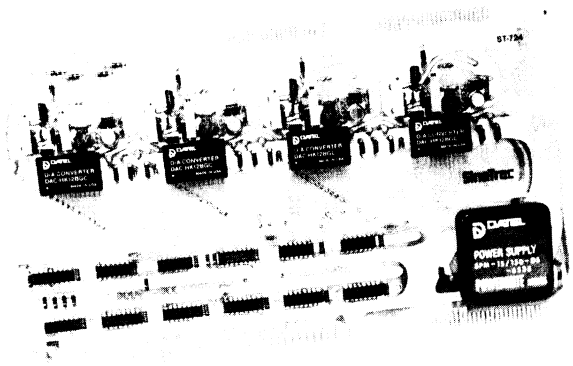
TYPICAL ST-705 MOUNTING IN A NEMA HOUSING



SineTrac ST-724
4-Channel D/A and Current Loop Board for MULTIBUS Microcomputers

FEATURES

- **4 D/A channels using 12-bit Hybrid Converters with Input Registers**
- **Accurate to .05% of Full Scale Reading**
- **Memory-mapped, with user-selectable Base Address**
- **Complete hardware and software compatibility with Multibus and SBC-series Microcomputers**
- **Pin-for-pin replacement for iSBC-724. Uses identical programming and register assignments to iSBC-711/732 and ST-711/732 A/D-D/A boards**
- **Works directly from Intel RMX Software**
- **Includes 4 externally excited 4 to 20 mA industrial current loop amplifiers.**
- **Pin-selectable Transfer Acknowledge (Xack/) Delay—ensures compatibility with different memory speeds**
- **On-board DC/DC power converter generates ±15 Vdc from +5 Vdc computer bus**



INTRODUCTION

The ST-724 Analog Output board extends DATEL's SineTrac family of slide-in computer peripherals to a variety of industrial and instrumentation applications. It provides 4 channels of D/A conversion, each with 12 binary bits of resolution for an overall accuracy to within .05% FSR. The ST-724 is fully hardware and software compatible with the popular MULTIBUS series of microcomputers—it is a pin-for-pin replacement for the iSBC-724. And, the ST-724 is significantly less expensive than other boards with comparable features.

The ST-724 is memory mapped—it appears to the host computer as eight consecutive locations in memory. The board base address is factory set to F7Ø8 but may be reassigned by the user anywhere in memory. The ST-724 also features an adjustable Transfer Acknowledge Delay (XACK/Delay). The ST-724 generates a Transfer Acknowledge signal in response to memory write commands from the system computer. The XACK/Delay circuitry permits a delay of this signal, to ensure compatibility with the host computer.

Digital inputs to the ST-724 may be set for offset binary or 2's complement (bipolar) coding or for straight binary (unipolar). Outputs from ±5V, ±10V, 0→+5V and 0→+10V DC permit the ST-724 to interface with a variety of process receivers, proportional controllers, or recorders. A 4 to 20 mA current loop is also provided which permits the board to be used in electrically noisy industrial environments. All outputs may be shorted to ground without damage.

Power to the ST-724 comes from the host computer's +5V power bus. An on-board DC-to-DC converter generates ±15V for the analog output circuitry.

DESCRIPTION

Input to the ST-724 is from the host computer data bus. Since the Intel Multibus provides only 8 binary bits of data per memory word, and the D/A converters on the ST-724 require 12 binary bits, two memory bytes are required for each conversion. The 4 least significant bits are transmitted first, (for DAC Φ, at the base memory address) and are latched into a 4-bit register. The next data byte (base address +1) contains the 8 MSB bits, and initiates a conversion.

D/A conversion is accomplished by DATEL's DAC-HK12BGC, a 12-bit hybrid unit with an input storage register and linearity to within ±½ LSB. The output of the converter is monotonic, having a differential nonlinearity of ±½ LSB maximum. Offset zero error on each channel has been adjusted to zero prior to shipping the board; pots on the board permit recalibration of zero or offset settings.

continued

Zero temperature coefficient (unipolar outputs only) for the converter is less than ±5 ppm/°C of Full Scale Reading. Offset temperature coefficient (bipolar outputs only) is within ±10 ppm/°C of FSR. Maximum gain tempco measures ±20 ppm/°C of FSR. DAC settling time is 4 μsec maximum (to within ½ LSB of value), and slew rate is 20V/μsec.

The voltage output ranges from the ST-724 board are jumper selectable and have an output impedance of 50 milliohms. Maximum available current on the voltage outputs is ±5mA. The ST-724 also provides voltage to current converters for each of its four D/A channels.

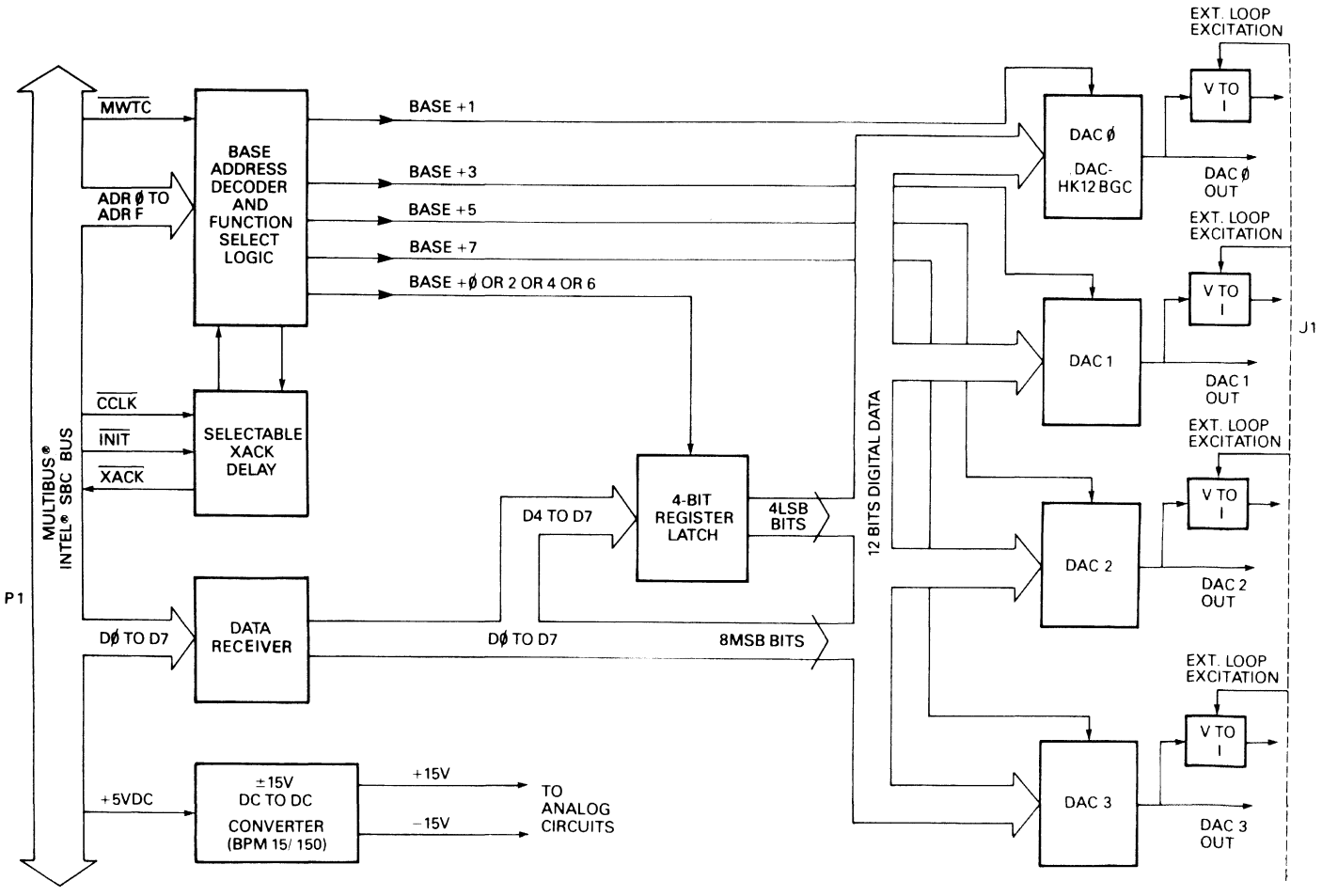
The current output option is jumper-selected by the user, and requires a user-supplied external excitation source (+18 to +30 Vdc).

The ST-724 is a memory-mapped device which occupies 8 consecutive memory locations. The starting (base) address is set at the factory to F7Ø8. However, the user may reposition this base address anywhere up to FFF8 in the host computer's memory by reconfiguring jumpers on the ST-724 board.

The selectable Transfer Acknowledge Delay Circuit (XACK/Delay) provides 16 delays from .05 to 1.5 μsec which may be jumper-programmed by the user.

The overall size of the ST-724 is 12.0"W × 6.75"D × 0.5"H (305 × 172 × 13 mm). Multiple ST-724 boards may be installed in adjacent card slots if used in a standard (.60" spacing) Intel card cage. The ST-724 weighs 18 ounces (.51 kg). It should be operated in an ambient temperature from 0 to +55°C, with relative humidity from 10% to 95% (non-condensing), and from 0 to 15,000 ft (0 to 4600m) in altitude. The board may be stored at temperatures from −25°C to +85°C. The ST-724 is powered from the host computer bus's +5 Vdc supply, and draws 1.5A.

ST-724
BLOCK DIAGRAM
4-Channel D/A



DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

SPECIFICATIONS

Typical at +25°C, dynamic conditions, unless otherwise specified

D/A ANALOG OUTPUT

Number of Channels. . 4 D/A channels

Channel Expansion. . . Indefinite channel expansion by separate, stand-alone ST-724 boards, each with a different base address; limited by available card slots, and power supply current.

Full Scale Output Ranges. . . . . ±10V (standard), ±5V, 0→+10V, 0→+5V, 4-20 mA (Current Loop) — Jumper Selectable by User

(The user must reassign jumpers to achieve ranges other than ±10V, offset binary)

Digital Input Coding. . . Straight Binary (standard), Offset Binary, 2's Complement — Jumper Selectable by User

Output Impedance. . . . 50 Milliohms

Maximum Current Available on Voltage Outputs. . . . ±5 mA @ ±10V short-circuit-proof to ground

Zero Temperature Drift. . . . . (Unipolar Output only) Within ±5 ppm of FSR/°C

Offset Temperature Drift. . . . . (Bipolar Output only) Within ±10 ppm of FSR/°C

Gain Temperature Drift. . . . . Within ±20 ppm of FSR/°C

Settling Time. . . . . Maximum, 4 µsec to within ½ LSB of final value

Slew Rate. 20V/µsec

Power Supply Rejection. . . . . 54 dB to DC supply bus

ADDRESSING

Reserves a block of 8 memory locations, all successive to a jumper-selectable memory base address

CURRENT LOOP EXTERNAL EXCITATION VOLTAGE

+18V to +30VDC, regulated, user-supplied. (25 mA maximum/DAC)

PERFORMANCE

Non-linearity. . . . . ±½ LSB maximum

Differential Non-linearity. . . . . ±½ LSB maximum

Offset or Zero Error. . . Adjustable to zero using pot. Each channel individually adjustable.

PHYSICAL

Outline Dimensions. . . 12.00"W × 6.75"D × 0.50"H (304, 8 x 171, 5 x 12, 7 mm) ST-724 boards may be installed adjacent to each other in SBC card cages.

Weight. . . . . 18 ounces (.510 kg)

Operating Temperature Range. . . . . 0 to +55°C

Storage Temperature Range. . . . . −25°C to +85°C

Relative Humidity. . . . 10% to 95%, non-condensing

Altitude. . . . . 0 to 15,000 ft (4600m)

POWER CONSUMPTION

+5Vdc ±5/% @ 1.5A from computer bus (±15Vdc supplied from on-board DC/DC power converter.)

GENERAL

Compatibility. . . . . Pin-for-pin, cardguide, and program compatible with Multibus and SBC-series microcomputers. A pin-for-pin replacement for the SBC-724.

Connector . . . . . Dual 25-pin PCB, 0.1" centers

ORDERING GUIDE

MODEL	DESCRIPTION
ST-724	4 Channel, Multibus-Compatible D/A Board
31-2076040	Edge Connector, J1, Spare (One Included with Board) (PCB to solder tab)
UM-ST-724	ST-724 User Manual (One included with Board)

For 8 D/A channels, use Model ST-728.

INPUT DATA FORMAT

Since 12-bit D/A converters are used on the ST-724, and since the Intel Multibus provides for only 8-bits of data per memory word, two 8-bit bytes in two sequential memory words are necessary for each D/A conversion.

The LS Byte is loaded onto the board first and is stored in a 4-bit register until the MS Byte is loaded. Thus, the memory location of the LS Byte is always the lower of the two locations used for a given channel. Conversion begins as soon as the MS Byte is loaded; within 4 microseconds an analog signal appears at the board's output.

LEAST SIGNIFICANT BYTE

D7	D6	D5	D4	D3	D2	D1	D0
DAC BIT 9	DAC BIT 10	DAC BIT 11	DAC BIT 12 (LSB)	X	X	X	X

MOST SIGNIFICANT BYTE

DAC BIT 1 (MSB)	DAC BIT 2	DAC BIT 3	DAC BIT 4	DAC BIT 5	DAC BIT 6	DAC BIT 7	DAC BIT 8

X = Don't care

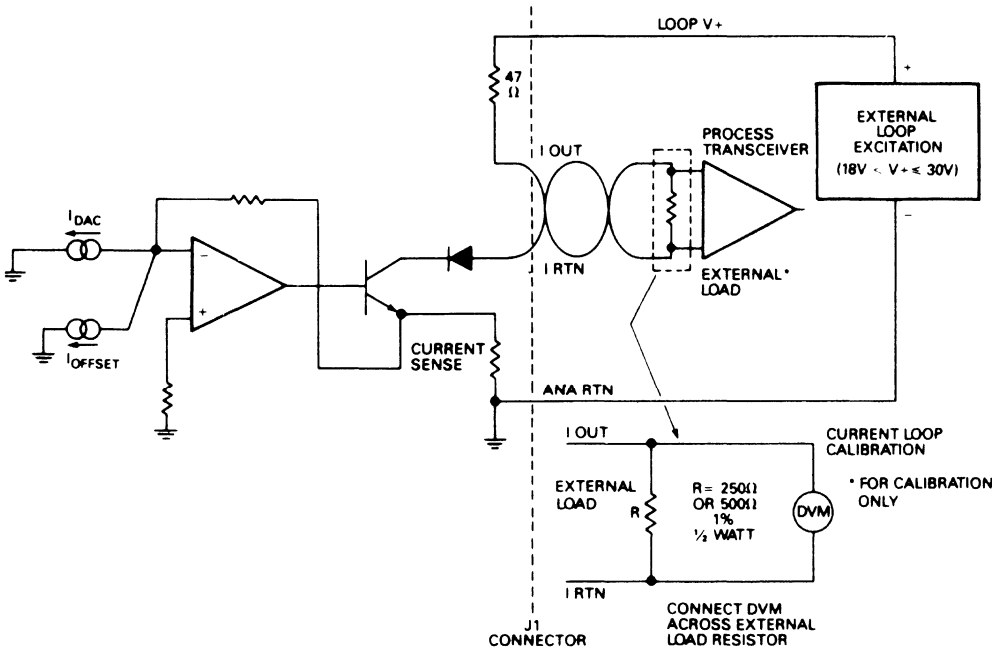
REGISTERS

The memory address bit function assignments are as follows. For an explanation of LSB and MSB Bytes, please see "Input Data Format".

ST-724 REGISTER ASSIGNMENTS

MEMORY ADDR.	FACTORY ASSIGNED MEM. ADDR.	FUNCTION
M+Ø	F7Ø8	Output LSB Byte for DAC Ø (Channel Ø)
M+1	F7Ø9	Output MSB Byte for DAC Ø (Channel Ø)
M+2	F7ØA	Output LSB Byte for DAC 1 (Channel 1)
M+3	F7ØB	Output MSB Byte for DAC 1 (Channel 1)
M+4	F7ØC	Output LSB Byte for DAC 2 (Channel 2)
M+5	F7ØD	Output MSB Byte for DAC 2 (Channel 2)
M+6	F7ØE	Output LSB Byte for DAC 3 (Channel 3)
M+7	F7ØF	Output MSB Byte for DAC 3 (Channel 3)

ST-724



Typical Current Loop Wiring

D/A CALIBRATION PROCEDURE

Calibration of the ST-724 should be performed every 90 days or whenever the Analog Output Range jumpers are reconfigured. More frequent calibration may be indicated in adverse operating conditions. The Diagnostic program supplied with the ST-724 was written as part of the calibration procedure.

1. Set the board jumpers for the desired output range: 0→+5V, 0→+10V, 4→20 mA, ±5V, or ±10V. See "Output Range Selection" for details.
2. Connect a digital voltmeter (Fluke 8800A or equivalent) to the outputs of Channel Ø (DAC Ø). For voltage ranges, measure between "V OUT" and "ANA RTN". For current ranges the user must supply a precision 250Ω or 500Ω resistor; voltage measurements are then made across this resistor (see Note 1, bottom of Calibration Table).
3. Using the Diagnostic program, select the "Calibration Test", Call Key "C".
4. The teletypewriter will respond by printing out:
   CALIBRATION TEST
   CHANNEL-
5. Enter character "Ø" to select Channel Ø (DAC Ø)
   CHANNEL- Ø
   HEX DATA
6. Making reference to the Calibration Table, enter the hex code for the −Full Scale output voltage (or current), then enter a Carriage Return. Adjust the OFFSET potentiometer, until the reading on the DVM corresponds to the −Full Scale reading from the table.
7. Refer again to the Calibration Table, and enter the hex code for + Full Scale voltage or current. Adjust the GAIN potentiometer until the reading on the DVM is the + Full Scale voltage as indicated in the table.
8. Repeat steps 6 and 7.
9. Calibration for Channels 1, 2, and 3 (DAC's 1, 2 & 3) is the same as for Channel Ø.
10. The complete calibration may now be checked using the Calibration Table. Any hex value on the table may be entered followed by a carriage return. The corresponding analog output should appear on the DVM.

CALIBRATION TABLE

ANALOG OUTPUT						4-DIGIT HEX INPUT	
UNIPOLAR (STRAIGHT BINARY)				BIPOLAR (OFFSET BINARY OR 2'S COMPLEMENT		STRAIGHT OR OFFSET BINARY - NO SIGN EXTENSION	2'S COMPLEMENT WITH SIGN EXTENSION
VOLTAGE		4→20 mA CURRENT[1]					
0→+5V	0→+10V	500Ω LOAD LOOP V+>18V	250Ω LOAD LOOP V+>15V	±5V	±10V		
4.9988V	9.9976V	9.9980V	4.9990V	4.9976V	9.9951V	FFFØ	7FFØ
4.9976V	9.9951V	9.9961V	4.9980V	4.9951V	9.9902V	FFEØ	7FEØ
4.9951V	9.9902V	9.9922V	4.9961V	4.9902V	9.9805V	FFCØ	7FCØ
4.9902V	9.9805V	9.9844V	4.9922V	4.9805V	9.9609V	FF8Ø	7F8Ø
4.9805V	9.9609V	9.9687V	4.9844V	4.9609V	9.9219V	FFØØ	7FØØ
4.9609V	9.9219V	9.9375V	4.9687V	4.9219V	9.8437V	FEØØ	7EØØ
4.9219V	9.8437V	9.8750V	4.9375V	4.8437V	9.6875V	FCØØ	7CØØ
4.8437V	9.6875V	9.7500V	4.8750V	4.6875V	9.3750V	F8ØØ	78ØØ
4.6875V	9.3750V	9.5000V	4.7500V	4.3750V	8.7500V	FØØØ	7ØØØ
4.3750V	8.7500V	9.0000V	4.5000V	3.7500V	7.5000V	EØØØ	6ØØØ
3.7500V	7.5000V	8.0000V	4.0000V	2.5000V	5.0000V	CØØØ	4ØØØ
2.5000V	5.0000V	6.0000V	3.0000V	0.0000V	0.0000V	8ØØØ	ØØØØ
1.2500V	2.5000V	4.0000V	2.0000V	−2.5000V	−5.0000V	4ØØØ	CØØØ
0.6250V	1.2500V	3.0000V	1.5000V	−3.7500V	−7.5000V	2ØØØ	AØØØ
0.3125V	0.6250V	2.5000V	1.2500V	−4.3750V	−8.7500V	1ØØØ	9ØØØ
0.1563V	0.3125V	2.2500V	1.1250V	−4.6875V	−9.3750V	Ø8ØØ	88ØØ
0.0781V	0.1563V	2.1250V	1.0625V	−4.8437V	−9.6875V	Ø4ØØ	84ØØ
0.0391V	0.0781V	2.0625V	1.0312V	−4.9219V	−9.8437V	Ø2ØØ	82ØØ
0.0196V	0.0391V	2.0312V	1.0156V	−4.9609V	−9.9219V	Ø1ØØ	81ØØ
0.0098V	0.0196V	2.0156V	1.0078V	−4.9805V	−9.9609V	ØØ8Ø	8Ø8Ø
0.0049V	0.0098V	2.0078V	1.0039V	−4.9902V	−9.9805V	ØØ4Ø	8Ø4Ø
0.0024V	0.0049V	2.0039V	1.0020V	−4.9951V	−9.9902V	ØØ2Ø	8Ø2Ø
0.0012V	0.0024V	2.0020V	1.0010V	−4.9976V	−9.9951V	ØØ1Ø	8Ø1Ø
0.0000V	0.0000V	2.0000V	1.0000V	−5.0000V	−10.0000V	ØØØØ	8ØØØ

Note 1: Both the 250Ω and the 500Ω resistors (.1% precision) provide 4 to 20 mA output. The current output circuit is calibrated in terms of voltage since most digital multimeters provide greater resolution and accuracy on voltage measurements than on current.

The voltages listed are those measured across a 250Ω or a 500Ω precision resistor, connected between "I RTN" and "I OUT" on any DAC output. A user-supplied DC regulated voltage, V+ ($+15V < V+ \leq +30V$ for 250Ω resistor, $+18V < V+ \leq +30V$ for 500Ω resistor; 25 mA max) is required for current output and calibration, and should be connected to "V + LOOP". The supply providing V+ should be grounded at "ANA RTN".

BASE ADDRESS SELECTION

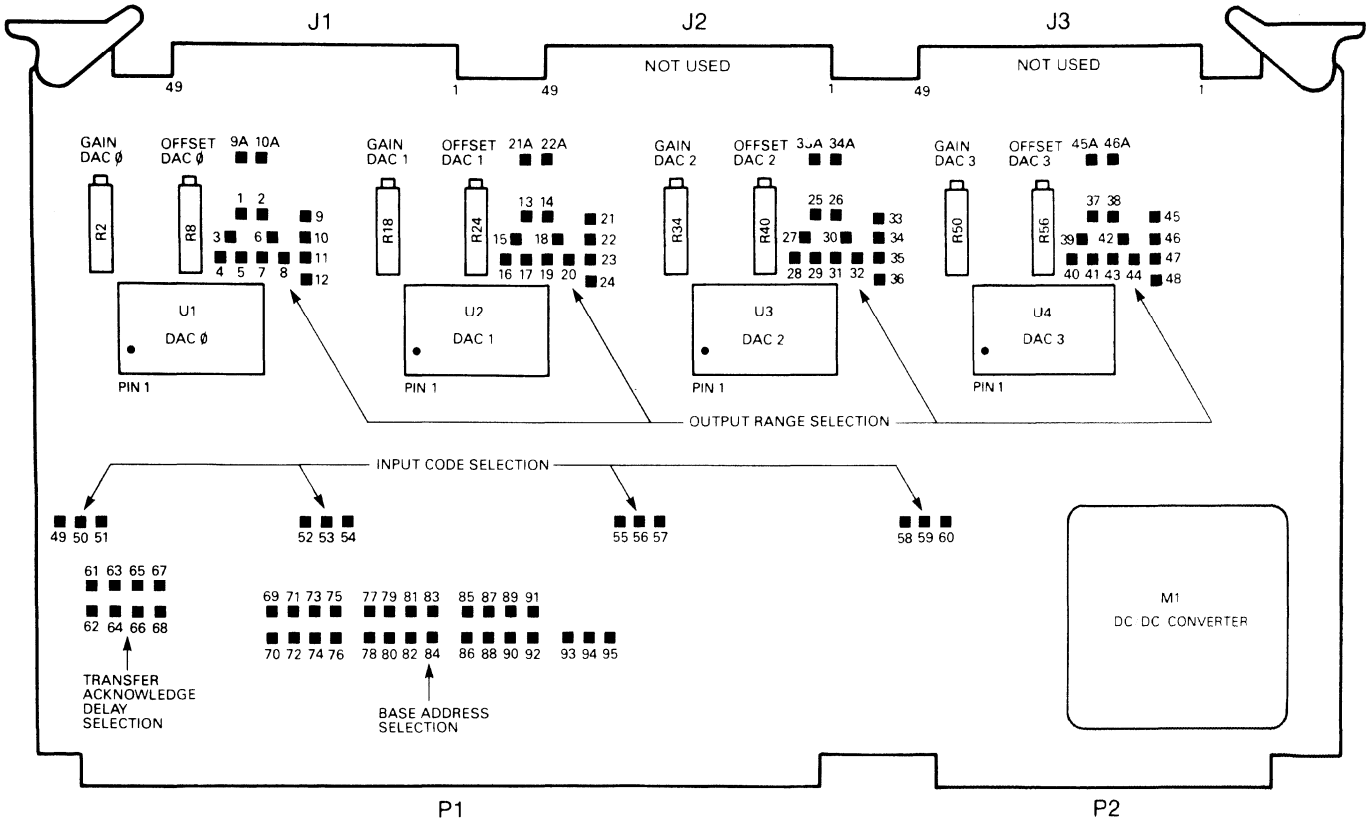
1. Select a base address, in hex, between ØØØØ and FFF8.
2. Write it in squares below opposite "Base Address, Hex".
3. Convert the hex code to binary by writing 1's and 0's in the appropriate boxes below (opposite "Hex Bit Weighting").
4. To set the base address, insert a jumper at each location opposite a "1". Please note that to obtain a "low" ("0") on bit 3, the jumper between 93 and 94 must be removed, and a jumper between 94 and 95 must be added.

BASE ADDRESS HEX	(Ø to F)				(Ø to F)				(Ø to F)				(Ø or 8)
HEX BIT WEIGHTING	8	4	2	1	8	4	2	1	8	4	2	1	8
ADDRESS BIT #	F	E	D	C	B	A	9	8	7	6	5	4	3
JUMPERS IN FOR "1", OUT FOR BIT "0"	69 to 70	71 to 72	73 to 74	75 to 76	77 to 78	79 to 80	81 to 82	83 to 84	85 to 86	87 to 88	89 to 90	91 to 92	93 to 94*

*For low on bit 3, remove 93 to 93 and add 94 to 95

BOARD LAYOUT

COMPONENT SIDE



DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

OUTPUT RANGE AND INPUT CODING SELECTION

The ST-724's 4 D/A output channels may be set independently for any of four voltage ranges or a single current output range. Full scale ranges of ±10V, ±5V, 0→+ 10V, 0→+5V, or 4→20 mA may be jumper-selected according to the chart below. Input digital coding may be offset binary, 2's complement, or straight binary on any channel. Again, refer to the chart below for details.

The ST-724 board is normally shipped with jumpers set for the ±10V output, and an offset binary input coding. Please note that whenever there is a change in output range on a given channel, that channel should be recalibrated.

INPUT CODE SELECTION JUMPERS

CODE	DAC Ø	DAC 1	DAC 2	DAC 3
UNIPOLAR OR OFFSET BINARY (STANDARD)	49-50	52-53	55-56	58-59
2'S COMPLEMENT	50-51	53-54	56-57	59-60

OUTPUT RANGE SELECTION JUMPERS

RANGE	DAC Ø	DAC 1	DAC 2	DAC 3
± 10V (STANDARD)	3-5 6-7	15-17 18-19	27-29 30-31	39-41 42-43
±5 V	3-5 6-8	15-17 18-20	27-29 30-32	39-41 42-44
0 to +10V	3-4 6-8	15-16 18-20	27-28 30-32	39-40 42-44
0 to +5V	1-2 3-4 6-8	13-14 15-16 18-20	25-26 27-28 30-32	37-38 39-40 42-44
4 to 20 mA CURRENT LOOP	9-10 11-12 9A-10A	21-22 23-24 21A-22A	33-34 35-36 33A-34A	45-46 47-48 45A-46A

TRANSFER ACKNOWLEDGE (XACK/) DELAY SELECTION

The ST-724 board generates a Transfer Acknowledge (XACK/) signal in response to Write commands from the host computer. It is sometimes desirable to delay this signal, in order to match the XACK/ signal to the host computer timing. A jumper selectable Transfer Acknowledge Delay (XACK/ delay) ranging from 50 nanoseconds to 1.5 microseconds is available in the ST-724.

The accuracy of the XACK/ delay is dependent in part on the duty cycle of the CCLK/ signal generated by the computer—shorter duty cycles result in greater accuracy. The delay time is advanced on the leading edge of CCLK/; XACK/ is generated on the trailing edge of CCLK/.

Please refer to the table below for jumper configurations yielding different delay times.

XACK/ DELAY SELECTION

DELAY µsec.	JUMPERS			
*0.05	—	—	—	—
0.1	61-62	—	—	—
0.2	—	63-64	—	—
0.3	61-62	63-64	—	—
0.4	—	—	65-66	—
0.5	61-62	—	65-66	—
0.6	—	63-64	65-66	—
0.7	61-62	63-64	65-66	—
0.8	—	—	—	67-68
0.9	61-62	—	—	67-68
1.0	—	63-64	—	67-68
1.1	61-62	63-64	—	67-68
1.2	—	—	65-66	67-68
1.3	61-62	—	65-66	67-68
1.4	—	63-64	65-66	67-68
1.5	61-62	63-64	65-66	67-68

*Factory supplied configuration.

ANALOG OUTPUT CONNECTIONS

J 1

ETCH SIDE	PIN #'S		COMPONENT SIDE
NC	2	1	NC
NC	4	3	NC
NC	6	5	NC
NC	8	7	NC
NC	10	9	NC
NC	12	11	NC
NC	14	13	NC
NC	16	15	NC
NC	18	17	NC
NC	20	19	NC
NC	22	21	NC
DAC 3, V OUT	24	23	NC
DAC 3, I OUT	26	25	DAC 3, I RTN
DAC 3, LOOP V + IN	28	27	DAC 3, ANA RTN
DAC 2, V OUT	30	29	NC
DAC 2, I OUT	32	31	DAC 2, I RTN
DAC 2, LOOP V + IN	34	33	DAC 2, ANA RTN
DAC 1, V OUT	36	35	NC
DAC 1, I OUT	38	37	DAC 1, I RTN
DAC 1, LOOP V + IN	40	39	DAC 1, ANA RTN
DAC Ø, V OUT	42	41	NC
DAC Ø, I OUT	44	43	DAC Ø, I RTN
DAC Ø, LOOP V + IN	46	45	DAC Ø, ANA RTN
POWER COMMON	48	47	POWER COMMON
−15 REF. VOLT. OUT*	50	49	+15 REF. VOLT. OUT*

*Not intended to power external circuitry; 1 mA max.

Contact DATEL for:

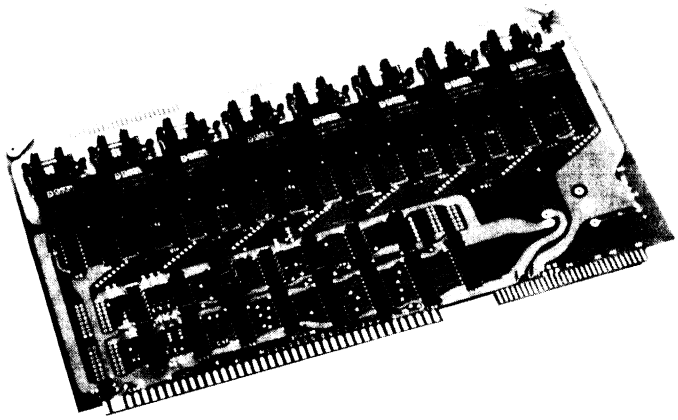
- **Data Acquisition & Control Boards**
- **Panel Meters, Printers, & Calibrators**
- **Data Conversion Components**
- **Power Supplies**

Dial
1-800-233-2765
for
Immediate Assistance

SineTrac ST-716
16-Bit D/A Board for MULTIBUS ISBC-80 Microcomputers

FEATURES

- **4 or 8 D/A channels, 16-bit resolution**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Accurate to 0.005% of Full-Scale reading**
- **Complete hardware and software compatibility with MULTIBUS and ISBC-Series microcomputers**
- **24-bit addressing**
- **Memory-mapped, with user-selectable base address**
- **Three user-selectable output ranges available: ±5 V dc, 0 to +10 V dc, and ±10 V dc**
- **Selectable Transfer Acknowledge delay (XACK/) ensures compatibility with different memory speeds**



DATEL'S SineTrac ST-716 D/A BOARD PROVIDES END USERS AND OEM's WITH A MEANS OF PRODUCING HIGH RESOLUTION ANALOG OUTPUTS FROM THEIR MULTIBUS AND ISBC MICROCOMPUTERS, WITH 16 BITS OF RESOLUTION, THIS BOARD IS AN IDEAL CHOICE FOR PRECISION SERVO CONTROL AND SIMILAR APPLICATIONS.

GENERAL DESCRIPTION

The ST-716 provides 4 or 8 channels of digital-to-analog (D/A) conversion with 16 bits of resolution. Overall accuracy is within .005% of full scale reading. Voltage range outputs are jumper-selectable to ensure the board's compatibility with popular process control and test instrumentation.

Like other SineTrac products, the ST-716 is fully hardware and software compatible with its host ISBC or MULTIBUS computer. All necessary address decoders, logic controls, and data receivers are built in. The user simply slides the ST-716 into an Intel-compatible card cage and wires the analog outputs. The ST-716 is then ready as a memory-mapped D/A peripheral. It is addressed by the host computer as 16 consecutive memory locations with a user-defined base address. This memory-mapped format permits virtually unlimited D/A channel expansion by using multiple ST-716's, each with a different base address.

A systems manual is shipped with each board, providing installation instructions, theory of operation, and engineering drawings.

Figure 1 is a simplified block diagram of the ST-716, with the 8 D/A channel circuitry for Model ST-716D shown within dashed lines. The ST-716 is pin-compatible with DATEL's ST-724, ST-728, ISBC-724, and ISBC-728 analog output boards. The 4-channel ST-716's are software-compatible with the ST-724's and ST-728's while the 8-channel ST-716's are software-compatible with the ST-728's.

Data inputs to the ST-716 are from the host computer's bus. Input coding is offset binary.

Each channel uses a DATEL Model DAC-HP16B (or DAC-HP16B-1), a 16-bit hybrid device which offers linearity to ±0.003% of Full-Scale reading. The output of the converter is monotonic to 14 bits between +10°C and +40°C. Offset error on each channel has been adjusted to zero prior to shipping the boards. Trim pots on the board permit recalibration of zero (or offset) and range setting. The converter settles in 15μS to within ±0.005% of FSR. Zero tempco is ±5 ppm of FSR/°C, and gain tempco is within ±20 ppm of FSR/°C.

The board's base address is factory set at 0F710. However, the user may relocate the board's address anywhere up to FFFF0 by rewiring a 20-pin DIP plug supplied with the board. The user may also extend the addressing to a full 24 bits by soldering jumpers into holes provided on the board adding four more bits. This would extend the addressing capability to FFFFF0 hex.

In order to make the ST-716 compatible with different speed CPU and memory systems, a Transfer Acknowledge delay (XACK/Delay) circuit is provided. The user enables 16 jumper-selectable delays from .05 to 1.5 microseconds.

The ST-716 is fully bus, card cage, and software compatible with the MULTIBUS. The board is 12″W x 6.75″D x 0.5″H (305 x 172 x 13 mm). Multiple ST-716 boards can mount in adjacent card slots when used with a standard, .60″ spacing Intel card cage. The ST-716C and ST-716D draw all their power from the MULTIBUS +5V line.

An on-board dc-to-dc converter provides the ±15V to drive the board analog output circuits. The St-716 weighs approximately 11.2 ounces (0,318 kg). It can operate over a temperature range of 0 to +55°C with relative humidity from 10 to 90% (non-condensing), and from 0 to 15,000 feet (0 to 4600m) in altitude.

Refer to Figure 2 for information regarding the location of all user-selectable jumpers for addressing, XACK/Delay, and output range selection.

ORDERING INFORMATION
SEE LAST PAGE

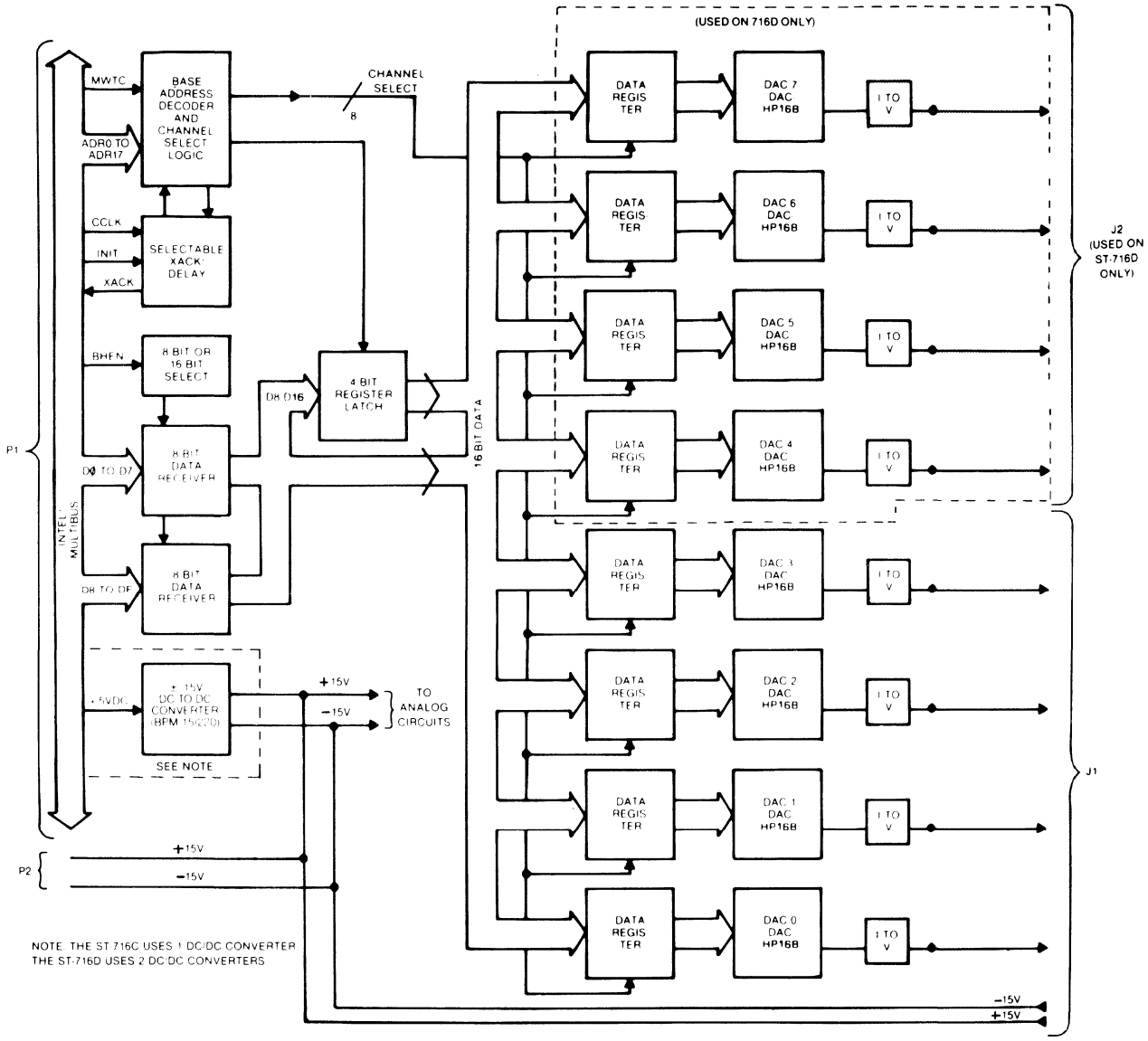


Figure 1. ST-716 Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, unless otherwise specified)

D/A ANALOG OUTPUT

Number of Channels
ST-716C . . . . . 4 D/A Channels with on-board dc-to-dc converter.
ST716D . . . . . 8 D/A channels with 2 on-board dc-to-dc converters.

Full Scale Output Ranges . . . . . ±5V, 0 to +10, ±10V dc
Digital Input Coding . . . . Offset Binary
Output Impedance . . . . . 50 Milliohms
Maximum Current Available on Voltage Outputs . . ±5 mA

Data Register Memory Mapping . . . . . Reserves a block of 16 consecutive memory locations

PERFORMANCE

Accuracy at +25°C . . . . . ±0.005% of FSR (includes noise and nonlinearity)
Setting Time . . . . . 10V change, 26 μSec. (to 0.005% FSR)
Power Supply Rejection . . ±0.002% FSR/%
Monotonicity . . . . . To 14 bits over +10°C to +40°C temp Range
Zero Temperature Drift (Unipolar Output Only) . . . Within ±5 ppm of FSR/°C
Offset Temperature Drift (Bipolar Output Only) . . ±8 ppm of FSR/°C
Gain Temperature Drift . . . Within ±20 ppm of FSR/°C

POWER CONSUMPTION

(From MULTIBUS +5 V dc, no load)

ST-716C . . . . . 2.0 Amps, typical
ST-716D . . . . . 4.2 Amps, typical

FUNCTIONAL SPECIFICATIONS (cont.)

PHYSICAL

Outline Dimensions . . . . . 12.00"W x 6.75"D x 0.50"H (304,8 x 171,5 x 12,7 mm) ST-716 boards may be installed adjacent to each other in SBC card cages with 0.60" spacing

Weight . . . . . 11.2 ounces (0,318 kg)

Operating Temperature Range . . . . . 0 to +55°C

Relative Humidity . . . . . 10% to 95%, non-condensing

Altitude . . . . . 0 to 10,000 ft.

SELECTION OF 8-BIT OR 16-BIT CPU's

The ST-716 board automatically changes to a 16-bit format when the BHEN/line on the MULTIBUS goes to zero volts (pin 27 of connector P1). A high input on BHEN/, consequently, sets the ST-716 for the 8-bit format.

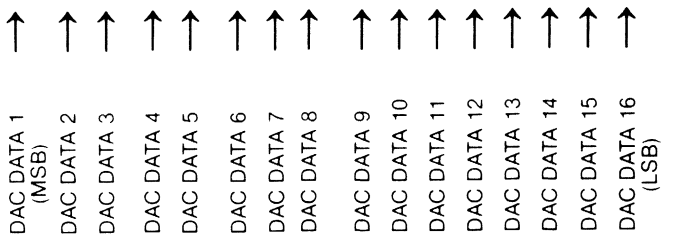
DATA FORMAT

The ST-716 requires 16 bits of digital data, input from the host computer, for a single digital-to-analog (D/A) conversion. Table 1 indicates how 8-bit and 16-bit CPU's format this data.

Note that 8-bit CPU's must transmit the 16 data bits in two bytes. The low byte contains the 8 least significant data bits; these are stored in a data register on the ST-716. The high byte contains the remaining 8 data bits. When the host transmits the high byte containing the 8 MSB's, the data register places the 8 LSB's also onto the selected DAC's input. Digital to-analog conversion then begins. Data transfer with a 16-bit CPU is somewhat simpler. All 16 data bits are transmitted as a single word. Data is loaded directly into the selected DAC, and a D/A conversion takes place.

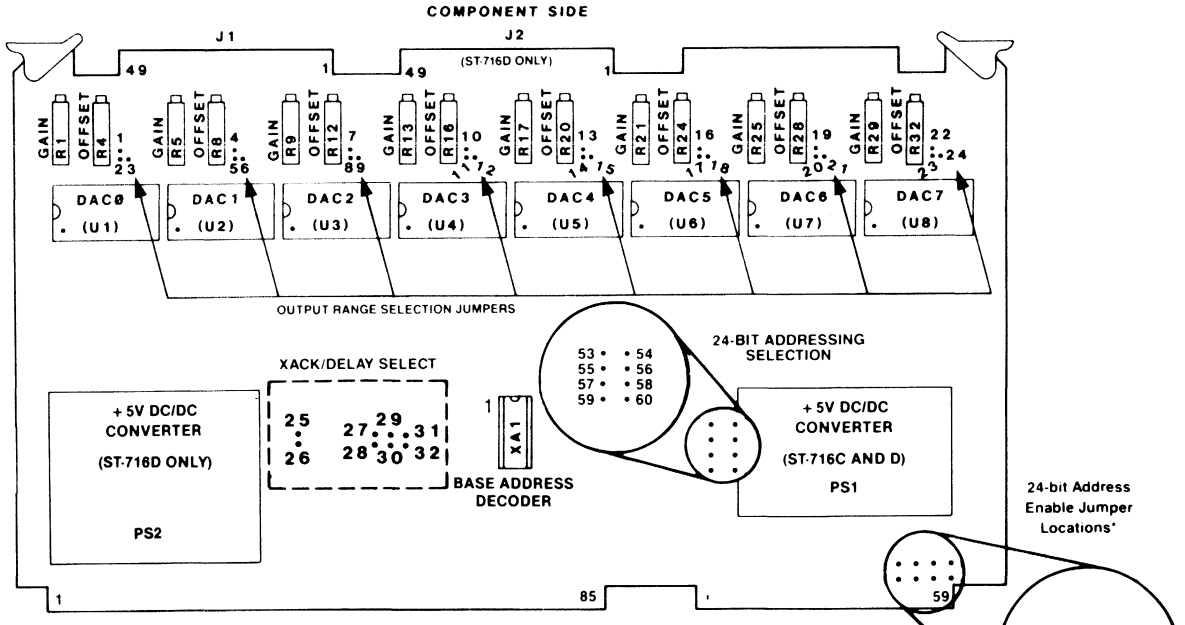
Table 1. Data Formats for 8- or 16-Bit CPU's

SINGLE WORD, 16-BIT CPU	
HIGH BYTE (8-BIT CPU) BASE + 1,3,5,7,9,B,D, or F	LOW BYTE (8-BIT CPU) BASE + 0, 2,4,6,8,A,C, or E
D15 D14 D13 D12 D11 D10 D9 D8	D7 D6 D5 D4 D3 D2 D1 D0



ST-716 REGISTER ASSIGNMENTS

Table 2 details the memory address assignments of the 16 memory locations the ST-716 occupies. Please note that when the ST-716 is used with 16-bit CPU's, every other (even-numbered) address location is used.



*User solders jumper wires between holes.
Jumper = Logic 1
No Jumper = Logic 0
See 24-Bit Addressing

OUTPUT VOLTAGE RANGE	JUMPER SELECTION							
	DAC0	DAC1	DAC2	DAC3	DAC4	DAC5	DAC6	DAC7
0-10V	2-3	5-6	8-9	11-12	14-15	17-18	20-21	23-24
±5V±10V	1-2	4-5	7-8	10-11	13-14	16-17	19-20	22-23

Figure 2. ST-716 Board Layout Drawing

BASE ADDRESS SELECTION

NOTE: The ST-716 may be used with both 8- and 16-bit microprocessors. Bits 10, 11, 12 and 13 are used or 20-bit addressing. Full 24-bit addressing would use these bits and address bits 14, 15, 16 and 17.

Use Table 3 as a worksheet to assign the base address.

Table 2. ST-716 Register Assignments

MEMORY ADDRESS (8-BIT CPU'S	FUNC-TION	REGISTER ASSIGNMENT	MEMORY ADDRESS (16-BIT) CPU'S
BASE + 0	WRITE	Output LSB Byte for DAC 0 (Channel 0)	BASE + 0)
BASE + 1	WRITE	Output MSB Byte for DAC 0 (Channel 0)	
BASE + 2	WRITE	Output LSB Byte for DAC 1 (Channel 1)	BASE + 2
BASE + 3	WRITE	Output MSB Byte for DAC 1 (Channel 1)	
BASE + 4	WRITE	Output LSB Byte for DAC 2 (Channel 2)	BASE + 4
BASE + 5	WRITE	Output MSB Byte for DAC 2 (Channel 2)	
BASE + 6	WRITE	Output LSB Byte for DAC 3 (Channel 3)	BASE + 6
BASE + 7	WRITE	Output MSB Byte for DAC 3 (Channel 3)	
BASE + 8	WRITE	Output LSB Byte for DAC 4 (Channel 4)	BASE + 8
BASE + 9	WRITE	Output MSB Byte for DAC 4 (Channel 4)	
BASE + A	WRITE	Output LSB Byte for DAC 5 (Channel 5)	BASE + A
BASE + B	WRITE	Output MSB Byte for DAC 5 (Channel 5)	
BASE + C	WRITE	Output LSB Byte for DAC 6 (Channel 6)	BASE + C
BASE + D	WRITE	Output MSB Byte for DAC 6 (Channel 6)	
BASE + E	WRITE	Output LSB Byte for DAC 7 (Channel 7)	BASE + E
BASE + F	WRITE	Output MSB Byte for DAC 7 (Channel 7)	

Procedure

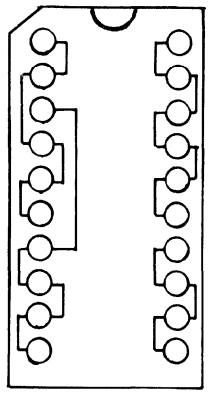
1. Select a base address, in hex, between 00000X and FFFFFX. Write all but the last digit in the boxes. (The last hex digit selects the 8 D/A channels, and cannot be preset).
2. Convert the hex code to binary by writing 1's and 0's in the boxes opposite "Hex Bit Weighting".
3. To set the ST-716 for a particular base address:

   Address bits 4 through 13: Connect the "1" pins together to pin 10 or 11 and the "0" pins together to pin 1 or 16, on DIP plug XA-1.
4. Address bits 0 through 3 select the 8 D/A channels and are not shown.
5. For 16-bit processors, bits 10, 11, 12 and 13 must be tied to pin 1.
6. XA-1 is a 20-pin DIP plug. (See Table 4)
7. Full 24-Bit addressing requires soldering jumper wires between etched holes provided on the ST-716 boards. See the ST-716 board component layout diagram for the location of these holes.

Table 4. Dip Plug XA-1 Pin Assignments

Set For Base Address of 0F700H

SIGNAL	PIN #	PIN #	SIGNAL
+5V	1	20	+5V
ADR 10	2	19	ADR 4
ADR C	3	18	ADR 5
ADR 11	4	17	ADR 6
ADR 12	5	16	ADR B
ADR 13	6	15	ADR 7
ADR F	7	14	ADR 8
ADR E	8	13	ADR 9
ADR D	9	12	ADR A
GND	10	11	GND



TOP VIEW

NOTES:

1. Address inputs to the ST-716 are low true. Tie pins to ground (Pin 10 or 11) for logic 1; tie them to +5V. (Pin 1 or 20) for a logic 0.
2. Etch holes exist on the board to assign logic levels to the additional four bits. Refer to the component layout diagram for the location of these holes.

Table 3. Base Address Selection

24-bit Addressing

20-bit Addressing

16-bit Addressing

BASE ADDRESS (HEX)	0 to F				0 to F				0 to F				0 to F				0 to F				x
HEX BIT WEIGHTING	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	•
ADDRESS BIT # HEX	17	16	15	14	13	12	11	10	F	E	D	C	B	A	9	8	7	6	5	4	
XA-1-PIN #'s/JUMPERS	NOT APPLICABLE SEE NOTE 1				Pin 6	Pin 5	Pin 4	Pin 2	Pin 7	Pin 8	Pin 9	Pin 3	Pin 16	Pin 12	Pin 13	Pin 14	Pin 15	Pin 17	Pin 18	Pin 19	

NOTES
1 Address bits 14, 15, 16 and 17 are enabled by placing jumpers across etched holes provided on the printed wiring board. See '24-Bit Addressing'
2 Boards are factory set for a base address of 00F10 hex

TRANSFER ACKNOWLEDGE (XACK/) DELAY SELECTION

The ST-716 board generates a Transfer Acknowledge (XACK/) signal in response to write commands from the host computer. It is sometimes desirable to delay this signal, in order to match the XACK/ signal to the host computer timing. The ST-716 has a jumper-selectable Transfer Acknowledge Delay (XACK/delay) ranging from 50 nanoseconds to 1.5 microseconds.

The accuracy of the XACK/delay is dependent in part on the duty cycle of the CCLK/signal generated by the computer, shorter duty cycles result in greater accuracy. The delay time is advanced on the leading edge of CCLK/; XACK/ is generated on the trailing edge of CCLK/.

Please refer to Table 5 for jumper configurations yielding different delay times.

OUTPUT RANGE CODING SELECTION

Datel ships the ST-716 boards with the full-scale output ranges configured as follows:

ST-716C1	± 5V dc
ST-716D1	0 to +10V dc
ST-716C2, D2	±10V dc

The particular jumper connections for individual DAC's appear in Table 6.

Tables 7 and 8 show the signals present on the output connectors of the ST-716.

Table 5. XACK/Delay Selection

DELAY µsec	JUMPERS			
*0.05	—	—	—	—
0.1	31-32	—	—	—
0.2	—	25-26	—	—
0.3	31-32	25-26	—	—
0.4	—	—	27-28	—
0.5	31-32	—	27-38	—
0.6	—	25-26	27-28	—
0.7	31-32	25-26	27-28	—
0.8	—	—	—	29-30
0.9	31-32	—	—	29-30
1.0	—	25-26	—	29-30
1.1	31-32	25-26	—	29-30
1.2	—	—	27-28	29-30
1.3	31-32	—	27-28	29-30
1.4	—	25-26	27-28	29-30
1.5	31-32	25-26	27-28	29-30

*Factory supplied configurations

Table 6. ST-716 Output Range Selection Jumpers

MODEL	RANGE	DAC 0	DAC 1	DAC 2	DAC 3	DAC 4	DAC 5	DAC 6	DAC 7
ST-716C2 ST-716D2	± 10V	1-2	4-5	7-8	10-11	13-14	16-17	19-20	22-23
ST-716C1	± 5V	1-2	4-5	7-8	10-11	13-14	16-17	19-20	22-23
ST-716D1	0 to + 10V	2-3	5-6	8-9	11-12	14-15	17-18	20-21	22-24

Table 7. J1 Analog Output Connections

WIRING SIDE	PIN #'S		COMPONENT SIDE
N/C	2	1	N/C
N/C	4	3	N/C
N/C	6	5	N/C
N/C	8	7	N/C
N/C	10	9	N/C
N/C	12	11	N/C
N/C	14	13	N/C
N/C	16	15	N/C
N/C	18	17	N/C
N/C	20	19	N/C
N/C	22	21	N/C
DAC 3, V OUT	24	23	DAC 3, ANA RTN
N/C	26	25	N/C
N/C	28	27	GND
DAC 2, V OUT	30	29	DAC 2, ANA RTN
N/C	32	31	N/C
N/C	34	33	GND
DAC 1, V OUT	36	35	DAC 1, ANA RTN
N/C	38	37	N/C
N/C	40	39	GND
DAC 0, V OUT	42	41	DAC 0, ANA RTN
N/C	44	43	N/C
N/C	46	45	GND
POWER COMMON	48	47	POWER COMMON
– 15V POWER[1]	50	49	+ 15V POWER[1]

NOTE: Pins 49 and 50 are outputs; 1 mA maximum (for reference only)

Table 8. J2 Analog Output Connections

WIRING SIDE	PIN #'S		COMPONENT SIDE
N/C	2	1	N/C
N/C	4	3	N/C
N/C	6	5	N/C
N/C	8	7	N/C
N/C	10	9	N/C
N/C	12	11	N/C
N/C	14	13	N/C
N/C	16	15	N/C
N/C	18	17	N/C
N/C	20	19	N/C
N/C	22	21	N/C
DAC 7, V OUT	24	23	DAC 7, ANA RTN
N/C	26	25	N/C
N/C	28	27	GND
DAC 6, V OUT	30	29	DAC 6, ANA RTN
N/C	32	31	N/C
N/C	34	33	GND
DAC 5, V OUT	36	35	DAC 5, ANA RTN
N/C	38	37	N/C
N/C	40	39	GND
DAC 4, V OUT	42	41	DAC 4, ANA RTN
N/C	44	43	N/C
N/C	46	45	GND
POWER COMMON	48	47	POWER COMMON
– 15V POWER[2]	50	49	+ 15V POWER[2]

NOTES:

1. J2 not used on 4 channel versions of ST-716.
2. Pins 49 and 50 are outputs; 1 mA maximum (for reference only)

24-BIT-ADDRESSING

For 16 or 20-bit addressing, Remove jumpers 53 through 68. For 24-bit addressing, install jumpers 61 to 62, 63 to 64, 65 to 66 and 67 to 68. Also install the following according to the desired address:

Address bit:	A17/	A16/	A15/	A14/
Jumper:	59-60	57-58	55-56	53-54

OPEN = "O", CLOSED = "1"

MSB Data Coding

Coding	Jumper
Straight or offset binary (non-inverted)	75 - 76
Two's complement bipolar (inverted MSB)	76 - 77

ORDERING INFORMATION

MODEL

ST-716 ___ ___

- 1 - ±5V dc, or 0 to +10V dc Output
- 2 - ±10V dc Output
- C-4 D/A Channels
- D-8 D/A Channels

ACCESSORIES

Part Number	Description
31-20760040	Edge Connector for J1, J2, (Two supplied)

SineTrac ST-728
D/A Board for MULTIBUS Microcomputers

FEATURES

- **4 or 8 D/A channels, 12 bit resolution**
- **Compatible with both 8 and 16 bit CPU's (8 or 16 bit data transfer)**
- **16, 20-, or 24-Bit addressing**
- **Accurate to 0.05% of Full Scale Reading**
- **Complete hardware and software compatibility with MULTIBUS and iSBC-Series microcomputers**
- **Memory-mapped, with user selectable Base Address**
- **Three user-selectable input data codes: Straight Binary, Offset Binary, or Two's Complement**
- **Five user-selectable output ranges: ±5V dc, ±10V dc, 0 to +5V dc, 0 to +10V dc, and 4-20 mA current loop, individually selected for each channel**
- **Selectable Transfer Acknowledge Delay (XACK/) – ensures compatibility with different memory speeds**
- **ST-728A (4 D/A channels)**
  ST-728B (8 D/A channels)
  ST-728C (4 D/A channels, DC-to-DC **converter)**
  ST-728D (8 D/A channels, DC-to-DC **converter)**

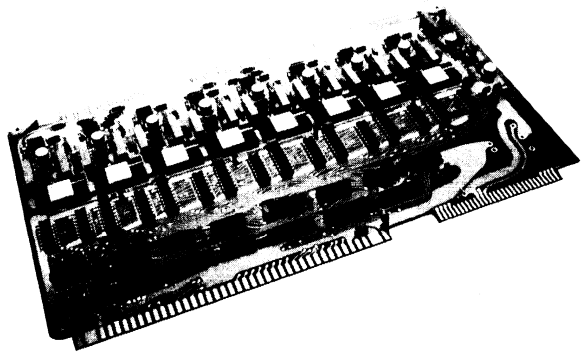
APPLICATIONS

- **Computer control of analog input chart recorders, process receivers, proportional controllers, actuators and displays**
- **Custom automatic test equipment, computer simulators, modelling systems, pattern generators, multi-channel Waveform generators**

INTRODUCTION

DATEL expands its range of MULTIBUS and SBC compatible analog output boards with the SineTrac ST-728. The ST-728 provides 4 or 8 channels of digital to analog (D/A) conversion with 12 bits of resolution. Overall accuracy is within ±.05% of full scale reading. To ensure the board's compatibility with popular process receiver, control, and test instrumentation, four voltages ranges, and a 4-20 mA current loop output are jumper selectable for each D/A channel.

Like other SineTrac products, the ST-728 is fully hardware and software compatible with its host SBC or MULTIBUS computer. All necessary address decoders, logic controls, and data receivers are built in. The user simply slides the ST-728 into an Intel compatible card cage and wires the analog outputs. The ST-728 is then ready as a memory-mapped D/A peripheral. It is addressed by the host computer as 16 consecutive memory locations with a user-locatable base address. This memory-mapped format permits unlimited D/A channel expansion by using multiple ST-728's, each with a different base address.



Compatible with: iSBC-80 Series
iSBC-86 Series

The ST-728 is pin compatible with the ST-724 and SBC-724 analog output boards (4 channel ST-728's are software compatible with ST-724's; 8-channel ST-728's look like two ST-724's). Unlike the ST-724, however, the ST-728 may be used with both 8-and 16-bit microprocessors. The BHEN/ line on the MULTIBUS sets the ST-728's address decoders and data latches for compatibility with 8- or 16-bit computers.

A systems manual is shipped with each board, which provides a source listing of the Diagnostic as well as installation instructions, theory of operation, and engineering drawings.

GENERAL DESCRIPTION

Data inputs to the ST-728 are from the host computer's bus. Input coding may be straight binary, offset binary, or two's complement, and is selected by jumper plugs on the board.

The MULTIBUS BHEN/ line is used to set the ST-728's address and data decoding for compatibility with 8 to 16 bit CPU's. In the 8 bit mode, the twelve bits of data required for D/A conversion are acquired in two bytes. The lower byte contains the four lower data bits, and is loaded into a storage register for each D/A channel on the ST-728. The next data byte contains the 8 higher bits. Upon converion, the 8 MSB's and the 4 stored bits are loaded simultaneously into the DAC. In the 16-bit mode, all twelve data bits are transferred in a single byte.

Prior to being converted, the digital data is held in a storage register. Enabling the register loads the data into the digital to analog converter (DAC), and a conversion proceeds.

Each channel uses a 12-bit monolithic D/A device which of-

fers linearity to ±1/2 LSB of full scale reading. The output of the converter is monotonic, having a differential nonlinearity of ±1/2 LSB maximum. Offset error on each channel has been adjusted to zero prior to shipping the boards. Trim pots on the board permit recalibration of zero (or offset) and range settings using the supplied Diagnostic program. The converter settles in 400 nS to within 1/2 LSB of it final value. Zero tempco is ±2 ppm of FSR/°C, and gain tempco is within ±10 ppm of FSR/°C.

The output of each DAC is fed to its own I-to-V conversion amplifier. A total of 4 voltage output ranges may be jumper-selected by the user: ±5V and ±10V bipolar; and 0 to +5V or 0 to +10V single-ended. In addition, a V to I converter circuit is included for each D/A output channel. 4-20 mA output, usable with an output load from 0 to 500 Ω, is also jumper-selectable.

The current output requires an external excitation source – a +18V to + 30V dc regulated supply, capable of 25 mA per D/A channel, must be provided. Voltage and current output ranges on the ST-728 are selected independently for each channel, permitting a mix of different voltage or current outputs on a single board.

The ST-728 is a memory-mapped peripheral occupying 16 consecutive locations in the host computer's memory. The board's base address is factory set at 0F700[1]. However, the user may relocate his address anywhere up to FFFFFØH.

In order to make the ST-728 compatible with different speed CPU and memory systems, a Transfer Acknowledge Delay (XACK/Delay) circuit is provided. 16 delays from 0.05 to 1.5 µS are jumper-selectable by the user.

The ST-728 is fully bus, card cage, and software compatible with the MULTIBUS and with Intel RMX software. The board is 12.0"W x 6.75"D x 0.5"H (305 x 172 x 13 mm). Multiple ST-728 boards may be mounted in adjacent card slots when used with a standard, 0.60" spacing Intel card cage.

The ST-728C draws all its power from the MULTIBUS +5V line. An on-board DC-to-DC converter provides the ±15 to drive the board's analog output circuits. The ST-728A and ST-728B do not have a DC-to-DC converter. They are powered from the +5V MULTIBUS line, and an external ±15V supply.

The ST-728 weighs approximately 11.2 ounces (0,318 kg). It can operate over a temperature range of 0 to +55°C with relative humidity from 10 to 90% (non-condensing), and from 0 to 15,000 feet (0 to 4600 m) in altitude.

INPUT DATA FORMAT AND REGISTER ASSIGNMENTS

DATA FORMAT

The ST-728 requires 12 bits of digital data, input from the host computer for single digital to analog (D/A) conversion. The chart below indicates how 8-bit and 16-bit CPU's format this data.

SINGLE BYTE, 16-BIT CPU

HIGH BYTE (8-bit CPU) BASE +1, 3, 5, 7, 9, B, D, or F	LOW BYTE (8-bit CPU) BASE +2, 4, 6, 8, A, C, or E
D15 D14 D13 D12 D11 D10 D9 D8	D7 D6 D5 D4 D3 D2 D1 D0

Note that 8-bit CPU's must transit the 12 data bits in two bytes. The low byte contains the four least significant data bits: these are stored in a data register on the ST-728. The high byte contains the remaining 8 data bits. When the high byte is transmitted, all twelve bits of data - the 4 LSB's stored in a register and the 8 MSB's coming from the host computer - are loaded into the input of the selected DAC on the ST-728, and D/A conversion proceeds. Data transfer with a 16-bit CPU is somewhat simpler. All twelve data bits are transmitted in a single word. Data is loaded directly into the selected DAC, and a D/A conversion takes place.

SELECTION OF 8-BIT OR 16-BIT CPU'S

The ST-728 board automatically changes to a 16-bit format when the BHEN/ line on the MULTIBUS goes to zero volts (pin 27 of the connector P1). A high input on BHEN/, consequently, sets the ST-728 for the 8-bit format.

ST-728 REGISTER ASSIGNMENTS

The following chart details the memory address assignments of the 16 memory locations the ST-728 occupies. Please note that when the ST-728 is used with 16-bit CPU's, every other (even-numbered) address location is used.

ST-728 REGISTER ASSIGNMENTS

MEMORY ADDRESS (8-bit CPU's)	FUNCTION	REGISTER ASSIGNMENT	MEMORY ADDRESS (16-bit CPU's)
BASE +0	WRITE	Output LSB Byte for DAC 0 (Channel 0)	BASE +0
BASE +1	WRITE	Output MSB Byte for DAC 0 (Channel 0)	
BASE +2	WRITE	Output LSB Byte for DAC 1 (Channel 1)	BASE +2
BASE +3	WRITE	Output MSB Byte for DAC 1 (Channel 1)	
BASE +4	WRITE	Output LSB Byte for DAC 2 (Channel 2)	BASE +4
BASE +5	WRITE	Output MSB Byte for DAC 2 (Channel 2)	
BASE +6	WRITE	Output LSB Byte for DAC 3 (Channel 3)	BASE +6
BASE +7	WRITE	Output MSB Byte for DAC 3 (Channel 3)	
BASE +8	WRITE	Output LSB Byte for DAC 4 (Channel 4)	BASE +8
BASE +9	WRITE	Output MSB Byte for DAC 4 (Channel 4)	
BASE +A	WRITE	Output LSB Byte for DAC 5 (Channel 5)	BASE +A
BASE +B	WRITE	Output MSB Byte for DAC 5 (Channel 5)	

Write the low byte first.

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, unless otherwise specified)

D/A ANALOG OUTPUT

Number of Channels

ST-728A, C - 4 D/A Channels
ST-728B, D - 8 D/A Channels
Indefinite channel expansion by separate, stand-alone ST-728 boards, each with a different base address; limited by available card slots, and power supply current.

Full Scale Output Ranges

±10V (standard)	Jumper Selectable by User for each channel
±5V	
0 to +10V	
0 to +5V	
4-20 mA	

Digital Input Coding

Straight Binary	Jumper Selectable by User in 4-channel groups
Offset Binary (Standard)	
2's Complement	

Output Impedance
50 Milliohms
Maximum Current Available on Voltage Outputs
±5 mA @ ±10V short-circuit-proof to ground
Current Loop Load Resistance
0 to 500Ω
Current Loop External Excitation Voltage
+18V to +30V dc, regulated, user-supplied (25 mA/DAC, max.)

ADDRESSING

Reserves a block of 16 consecutive memory locations. Base address may be located by jumper selection anywhere in the host computer's memory on 16-byte boundaries.

PERFORMANCE

Accuracy at +25°C
±0.05% of FSR (includes noise and nonlinearity)
Linearity Error, max. ±1/2 LSB
Linearity Error, 0°C to +70°C ±1 LSB
Differential Linearity Error ±1/2 LSB
Monotonicity
Monotonic over 0 to +55 °C temp. range
Zero Temperature Drift
(Unipolar Output only) Within ±2 ppm of FSR/°C
Offset Temperature Drift
(Bipolar Output only) Within ±5 ppm of FSR/°C

Gain Temperature Drift
Within ±10 ppm of FSR/°C
Settling Time (Board)
5 µS to within 1/2 LSB of final value

PHYSICAL

Outline Dimensions
12.00"W x 6.75"D x 0.50"H (304,8 x 171,5 x 12,7 mm)
ST-728 boards may be installed adjacent to each other in SBC card cages with 0.60" spacing
Weight (ST-728B) 11.2 ounces (0,318 kg)
Operating Temperature Range 0 to + 55°C
Relative Humidity 10% to 95%, non-condensing
Altitude 0 to 15,000 ft

POWER CONSUMPTION

All ST-728 models use some +5V power from the MULTIBUS. The ST-728C (4 channels) has an on-board DC-DC converter, so that *all* board power comes from the +5V line on the MULTIBUS. The ST-728A (4 channels no DC-to-DC) and ST-728B (8 channels, no DC-to-DC) require external ±15V supplies, input to the board via connector P2. The chart below summarizes the ST-728 board power requirements.

	from +5V MULTIBUS	+15V (P2)	-15V (P2)
ST-728A	750 mA	140 mA (150 mA)	70 mA (90 mA)
ST-728B	1000 mA	110 mA (130 mA)	275 mA (300 mA)
ST-728C	1500 mA max.	N/A	N/A
ST-728D	2500 mA max.	N/A	N/A

Except as noted, current readings are:
typical, (with output load)
typical, without output load

GENERAL

Bus Compatibility
Pin-for-pin, card guide, and program compatible with MULTIBUS and SBC-series microcomputers.

CPU Compatibility
May be used with either 8-bit or 16-bit microprocessors.

ANALOG OUTPUT CONNECTIONS

J1 (DAC'S 0, 1, 2, 3)

WIRING SIDE	PIN #'S		COMPONENT SIDE
NO CONNECTION	2	1	NO CONNECTION
NO CONNECTION	4	3	NO CONNECTION
NO CONNECTION	6	5	NO CONNECTION
NO CONNECTION	8	7	DAC 3, REF RTN
NO CONNECTION	10	9	DAC 3, EXT REF
NO CONNECTION	12	11	DAC 2, REF RTN
NO CONNECTION	14	13	DAC 2, EXT REF
NO CONNECTION	16	15	DAC 1, REF RTN
NO CONNECTION	18	17	DAC 1, EXT REF
NO CONNECTION	20	19	DAC 0, REF RTN
NO CONNECTION	22	21	DAC 0, EXT REF
DAC 3, V OUT	24	23	DAC 3, ANA RTN
DAC 3, I RTN	26	25	DAC 3, I RTN
DAC 3, LOOP V+	28	27	GND
DAC 2, V OUT	30	29	DAC 2, ANA RTN
DAC 2, I OUT	32	31	DAC 2, I RTN
DAC 2, LOOP V+	34	33	GND
DAC 1, V OUT	36	35	DAC 1, ANA RTN
DAC 1, I OUT	38	37	DAC 1, I RTN
DAC 1, LOOP V+	40	39	GND
DAC 0, V OUT	42	41	DAC 0, ANA RTN
DAC 0, I OUT	44	43	DAC 0, I RTN
DAC 0, LOOP V+	46	45	GND
POWER COMMON	48	47	POWER COMMON
-15V POWER[1]	50	49	+15V POWER[1]

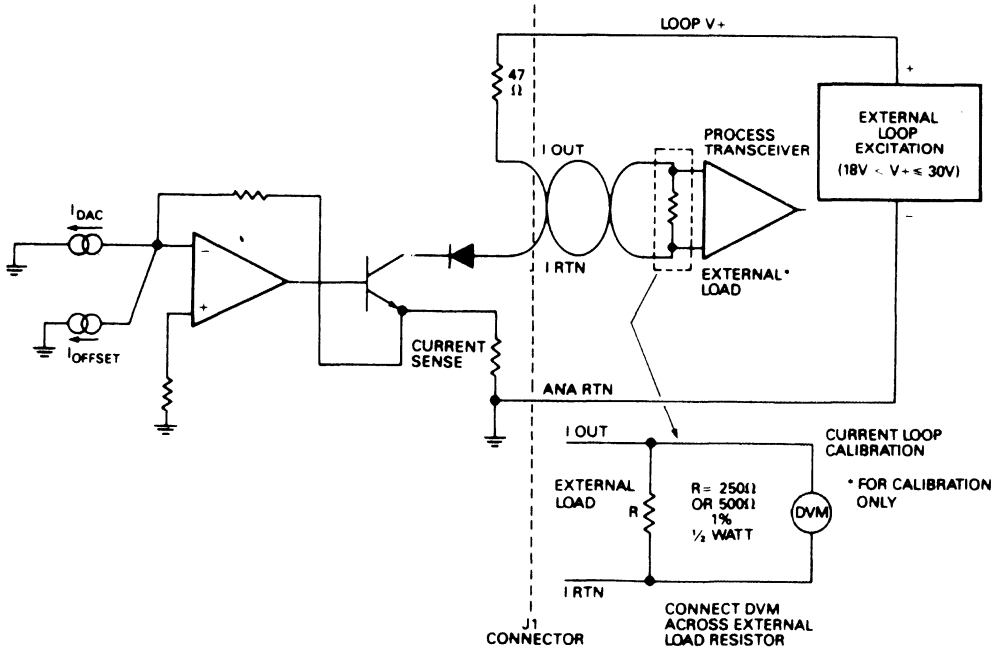
NOTE: 1. 49 & 50 are outputs; 1 mA max (for ref. only).

J2 (DAC'S 4, 5, 6, 7)[1]

WIRING SIDE	PIN #'S		COMPONENT SIDE
NO CONNECTION	2	1	NO CONNECTION
NO CONNECTION	4	3	NO CONNECTION
NO CONNECTION	6	5	NO CONNECTION
NO CONNECTION	8	7	DAC 7, REF RTN
NO CONNECTION	10	9	DAC 7, EXT REF
NO CONNECTION	12	11	DAC 6, REF RTN
NO CONNECTION	14	13	DAC 6, EXT REF
NO CONNECTION	16	15	DAC 5, REF RTN
NO CONNECTION	18	17	DAC 5, EXT REF
NO CONNECTION	20	19	DAC 4, REF RTN
NO CONNECTION	22	21	DAC 4, EXT REF
DAC 7, V OUT	24	23	DAC 7, ANA RTN
DAC 7, I OUT	26	25	DAC 7, I RTN
DAC 7, LOOP V+	28	27	GND
DAC 6, V OUT	30	29	DAC 6, ANA RTN
DAC 6, I OUT	32	31	DAC 6, I RTN
DAC 6, LOOP V+	34	33	GND
DAC 5, V OUT	36	35	DAC 5, ANA RTN
DAC 5, I OUT	38	37	DAC 5, I RTN
DAC 5, LOOP V+	40	39	GND
DAC 4, V OUT	42	41	DAC 4, ANA RTN
DAC 4, I OUT	44	43	DAC 4, I RTN
DAC 4, LOOP V+	46	45	GND
POWER COMMON	48	47	POWER COMMON
-15V POWER [2]	50	49	+15V POWER [2]

NOTES: 1. J2 not used on 4 channel versions of ST-728
2. 49 & 50 are outputs; 1 mA max (for ref. only).

ST-728



Typical ST-728 Current Loop Wiring

D/A CALIBRATION PROCEDURE (Performed with optional Diagnostic Program)

Calibration of the ST-728 should be performed every 90 days or whenever the Analog Output Range jumpers are reconfigured. More frequent calibration may be indicated in adverse operating conditions. The Diagnostic program listed in the ST-728 user manual was written as part of the calibration procedure. Please see the section entitled "Diagnostic Program".

1. Set the board jumpers for the desired output range: 0 to +5V, 0 to +10V, 4-20 mA, ±5V, or ±10V. See "Output Range Selection" for details.
2. Connect a digital voltmeter (Fluke 8800A or equivalent) to the outputs of Channel 0 (DAC 0). For voltage ranges, measure between "V OUT" and "ANA RTN". For current ranges the user must supply a precision 25Ω or 500Ω resistor; voltage measurements are then made across this resistor (see Note 1, bottom of Calibration Table.)
3. Using the Diagnostic program, select the "Calibration Test", Call Key "C".
4. The teletypewriter will respond by printing out:
   CALIBRATION TEST
   CHANNEL-
5. Enter character "0" to select Channel 0 (DAC 0)
   CHANNEL-0
   HEX DATA
6. Making reference to the Calibration Table, enter the hex code for the –Full Scale output voltage(or current), then enter a Carriage Return. Adjust the OFFSET potentiometer, until the reading on the DVM corresponds to the –Full Scale reading from the table.
7. Refer again to the Calibration Table, and enter the hex code for +Full Scale voltage or current. Adjust the GAIN potentiometer until the reading on the DVM is the +Full Scale voltage as indicated in the table.
8. Repeat steps 6 and 7.
9. Calibration for Channels 1 through 7 (DACs 1 through 7) is the same as for Channel 0.
10. The complete calibration may now be checked using the Calibration Table. Any hex value on the table may be entered followed by a carriage return. The corresponding analog output should appear on the DVM.

CALIBRATION TABLE

ANALOG OUTPUT						4-DIGIT HEX INPUT	
UNIPOLAR (STRAIGHT BINARY)				BIPOLAR (OFFSET OR 2'S COMPLEMENT)			
VOLTAGE		4-20mA CURRENT[1]				STRAIGHT OR OFFSET BINARY- NO SIGN EXTENSION	2'S COMPLEMENT WITH SIGN EXTENSION
0 TO +5V	0 TO +10V	500Ω LOAD LOOP V+>18V	200Ω LOAD LOOP V+>15V	±5V	±10V		
4.9988V	9.9976V	9.9980V	4.9990V	4.9976V	9.9951V	FFF0	7FF0
4.9976V	9.9951V	9.9961V	4.9980V	4.9951V	9.9902V	FFE0	7FE0
4.9951V	9.9902V	9.9922V	4.9961V	4.9902V	9.9805V	FFC0	7FC0
4.9902V	9.9805V	9.9844V	4.9922V	4.9805V	9.9609V	FF80	7F80
4.9805V	9.9609V	9.9687V	4.9844V	4.9609V	9.9219V	FF00	7F00
4.9609V	9.9219V	9,9375V	4.9687V	4.9219V	9.8437V	FE00	7E00
4.9219V	9.8437V	9.8750V	4.9375V	4.8437V	9.6875V	FC00	7C00
4.8437V	9.6875V	9.7500V	4.8750V	4.6875V	9.3750V	F800	7800
4.6875V	9.3750V	9.5000V	4.7500V	4.3750V	8.7500V	F000	7000
4.3750V	8.7500V	9.0000V	4.5000V	3.7500V	7.5000V	E000	6000
3.7500V	7.5000V	8.0000V	4.0000V	2.5000V	5.0000V	C000	4000
2.5000V	5.0000V	6.0000V	3.0000V	0.0000V	0.0000V	8000	0000
1.2500V	2.5000V	4.0000V	2.0000V	-2.5000V	-5.0000V	4000	C000
0.6250V	1.2500V	3.0000V	1.5000V	-3.7500V	-7.5000V	2000	A000
0.3125V	0.6250V	2.5000V	1.2500V	-4.3750V	-8.7500V	1000	9000
0.1563V	0.3125V	2.2500V	1.1250V	-4.6875V	-9.3750V	0800	8800
0.0781V	0.1563V	2.1250V	1.0625V	-4.8437V	-9.6875V	0400	8400
0.0391V	0.0781V	2.0625V	1.0312V	-4.9219V	-9.8437V	0200	8200
0.0196V	0.0391V	2.0312V	1.0156V	-4.9609V	-9.9219V	0100	8100
0.0098V	0.0196V	2.0156V	1.0078V	-4.9805V	-9.9609V	0080	8080
0.0049V	0.0098V	2.0078V	1.0039V	-4.9902V	-9.9805V	0040	8040
0.0024V	0.0049V	2.0039V	1.0020V	-4.9951V	-9.9902V	0020	8020
0.0012V	0.0024V	2.0020V	1.0010V	-4.9976V	-9.9951V	0010	8010
0.0000V	0.0000V	2.0000V	1.0000V	-5.0000V	-10.0000V	0000	8000

Note 1: Both the 250Ω and the 500Ω resistors (0.1% precision) provide 4 to 20 mA output. The current output circuit is calibrated in terms of voltage since most digital multimeters provide greater resolution and accuracy on voltage measurements than on current.

The voltages listed are those measured across a 250Ω or a 500Ω precision resistor, connected between "I RTN" and "I OUT" on any DAC output. A user-supplied DC regulated voltage, V+ (+15V < V+ ≤ +30V for 250Ω resistor, +18V < V+ ≤ +30V for 500Ω resistor; 25 mA max) is required for current output and calibration, and should be connected to "V+ LOOP". The supply providing V+ should be grounded at "ANA RTN".

TRANSFER ACKNOWLEDGE (XACK/) DELAY SELECTION

The ST-728 board generates a Transfer Acknowledge (XACK) signal in response to Write commands from the host computer. It is sometimes desirable to delay this signal in order to match the XACK/ signal to the host computer timing. A jumper selectable Transfer Acknowledge Delay (XACK/delay) ranging from 50 nanoseconds to 1.5 microseconds is available in the ST-728.

The accuracy of the XACK/delay is dependent in part on the duty cycle of the CCLK/ signal generated by the computer-shorter duty cycles result in greater accuracy. The delay time is advanced on the leading edge of CCLK/; XACK/ is generated on the trailing edge of CCLK/.

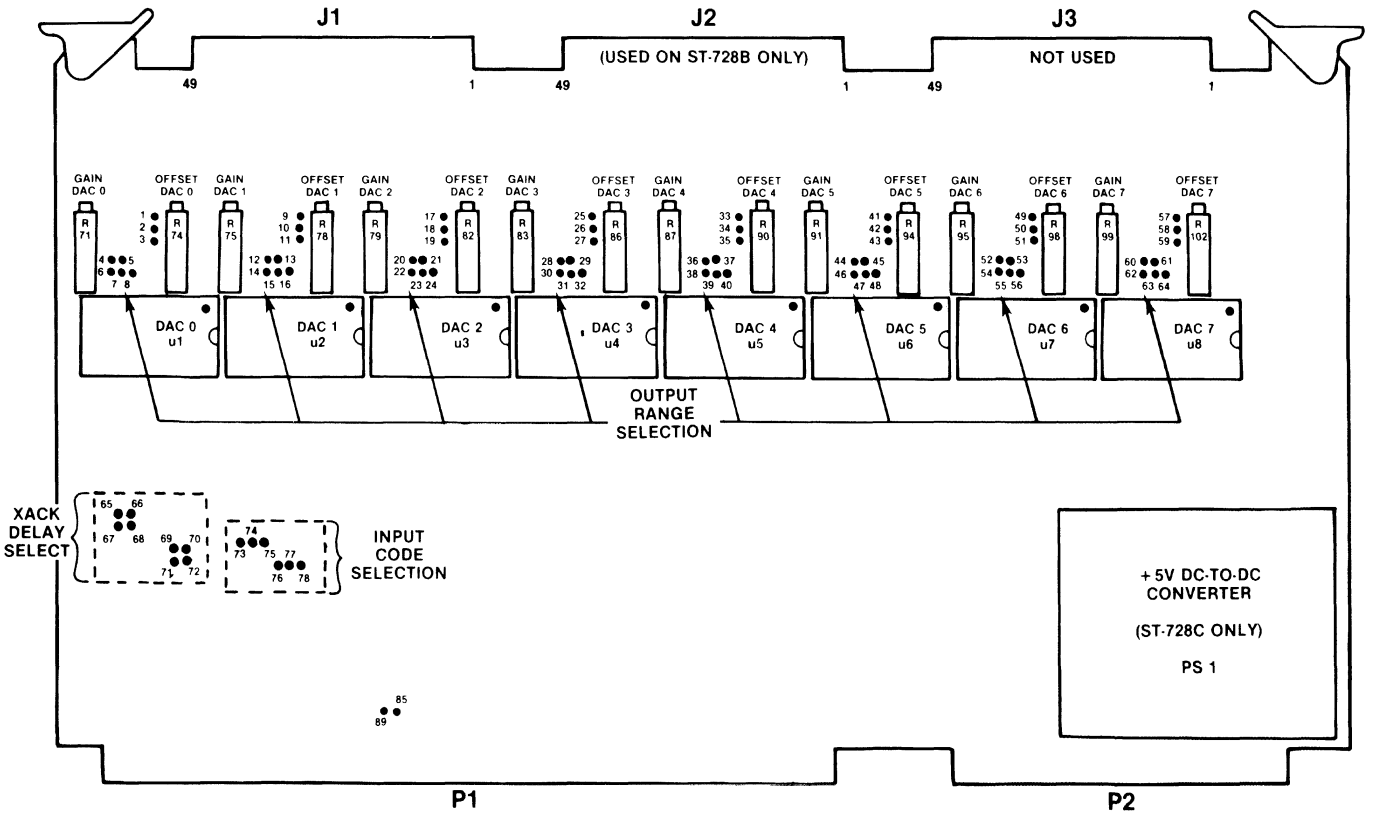
Please refer to the table for jumper configurations yielding different delay times.

XACK/ DELAY SELECTION

DELAY µsec.	JUMPERS			
0.05*	–	–	–	–
0.1	67-68	–	–	–
0.2	–	65-66	–	–
0.3	67-68	65-66	–	–
0.4	–	–	69-70	–
0.5	67-68	–	69-70	–
0.6	–	65-66	69-70	–
0.7	67-68	65-66	69-70	–
0.8	–	–	–	71-72
0.9	67-68	–	–	71-72
1.0	–	65-66	–	71-72
1.1	67-68	65-66	–	71-72
1.2	–	–	69-70	71-72
1.3	67-68	–	69-70	71-72
1.4	–	65-66	69-70	71-72
1.5	67-68	65-66	69-70	71-72

*Factory supplied configuration

COMPONENT SIDE



ST-728 Board Layout

BASE ADDRESS SELECTION

(For Assembly D–11625, Revision F or later)

Base Address (Hexadecimal)	[see note 2] (Ø to F)	(Ø to F)	(Ø to F)	(Ø to F)	(Ø to F)	* (Ø)
Hex bit weighing	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	
Address Bit (Hex)	17 16 15 14	13 12 11 10	F E D C	B A 9 8	7 6 5 4	3 - 0
Jumper (see note 1)	A A A A 17 16 15 14	A A A A 13 12 11 10	AF AE AD AC	AB AA A9 A8	A7 A6 A5 A4	

Note 1: Jumper Out =" Ø", Jumper In = "1".
* Address bits 3 - Ø are decoded by D/A channel addressing.

Note 2: For 24-bit addressing, install jumper 80-81. For 16- or 20-bit addressing, remove jumper 80-81.

Note 3: To control 8- or 16-bit transfers by detecting BHEN/, remove jumper 84-85. Install jumper 84-85 to ground BHEN/ (always low).

OUTPUT RANGE INPUT CODING SELECTION

The ST-728's D/A output channels may be set independently for any of four voltage ranges or a single current output range. Full scale ranges of ±10V, ±5V, 0 to +10V, 0 to +5V, or 4–20 mA may be jumper-selected according to the chart below. Input digital coding may be offset binary, 2's complement, or straight binary. Again, refer to the chart below for details.

The ST-728 board is normally shipped with jumpers set for the ±10V output, and an offset binary input coding. Please note that whenever there is a change in output range on a given channel, that channel should be recalibrated.

INPUT CODE SELECTION JUMPERS

CODE	DAC 0 TO DAC 3	DAC 4 TO DAC 7
Unipolar or Offset Bin. (Standard)	74-75	77-78
2's Complement	73-74	76-77

OUTPUT RANGE SELECTION JUMPER

RANGE	DAC 0	DAC 1	DAC 2	DAC 3	DAC 4	DAC 5	DAC 6	DAC 7
±10V	2-3	10-11	18-19	26-27	34-35	42-43	50-51	58-59
(Standard)	4-5	12-13	20-21	28-29	36-37	44-45	52-53	60-61
±5V	2-3	10-11	18-19	26-27	34-35	42-43	50-51	58-59
	4-6	12-14	20-22	28-30	36-38	44-46	52-54	60-62
0 to +10V	4-6	12-14	20-22	28-30	36-38	44-46	52-54	60-62
0 to +5V	4-6	12-14	20-22	28-30	36-38	44-46	52-54	60-62
	5-7	13-15	21-23	29-31	37-39	45-47	53-55	61-63
4 to 20 mA Current Loop	1-2	9-10	17-18	25-26	33-34	41-42	49-50	57-58
	7-8	15-16	23-24	31-32	39-40	47-48	55-56	63-64

ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
ST-728A2/24	4 D/A Channels, no DC-DC Converter (±15V dc, +5V dc power required)
ST-728B2/24	8 D/A Channels, no DC-DC Converter (±15V dc, +5V dc power required)
ST-728C2/24	4 D/A Channels, with DC-DC Converter (+5V dc power required)
ST-728D2/24	8 D/A Channels, with DC-DC Converter (+5V dc power required)
31-2076040	Edge Connector, J1 and J2, Spare
UM-ST-728	ST-728 Manual (Spare; one supplied with board)

Standard (2/24) versions include the current loop option. Versions without current loops(1/24) are available at lower cost for scheduled, quantity orders.

Contact DATEL for:

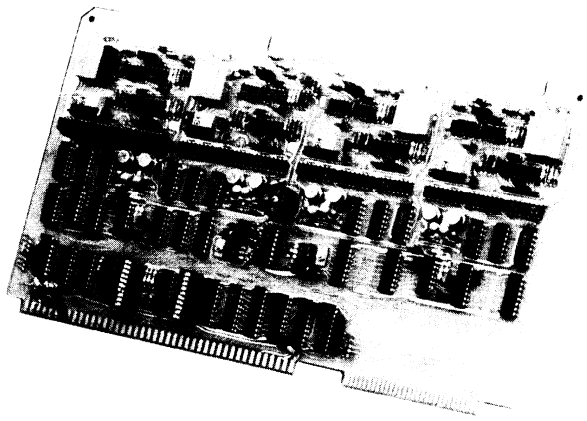
- **Data Acquisition & Control Boards**
- **Panel Meters, Printers, & Calibrators**
- **Data Conversion Components**
- **Power Supplies**

Dial
1-800-233-2765
for
Immediate Assistance

SineTrac ST-703
12-Bit, 4 Channel Isolated MULTIBUS D/A Board

FEATURES

- **4 D/A Channels using 12-bit monolithic converters**
- **300 VRMS Isolation, channel-to-channel and channel-to-bus**
- **Accurate to .05% of full-scale reading**
- **Uses identical programming and register assignments to SBC-711/732/724 and ST-711/732/724 boards**
- **Includes 4 externally excitation 4-20 mA current loop channels**
- **Memory mapped, with 24-, 20-, or 16-bit user selectable base address**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Complete hardware and software compatibility with MULTIBUS and SBC series microcomputers**



INTRODUCTION

DATEL expands its line of MULTIBUS and SBC compatible analog output boards with the SineTrac ST-703. The ST-703 provides 4 channels of isolated digital-to-analog (D/A) conversion with 12 bits of resolution. Overall voltage output accuracy is within ± .05% of full-scale range. To ensure the board's compatibility with popular process control and test instrumentation, four voltage ranges and a 4-20 mA current loop output are jumper selectable for each D/A channel.

Like other SineTrac products, the ST-703 is fully hardware-and-software-compatible with its host iSBC or MULTIBUS computer. All necessary address decoders, logic controls, and data receivers are built-in. The user installs the ST-703 into an Intel-compatible card cage and wires the analog outputs. The ST-703 is then configured as a memory-mapped peripheral which is addressed by the host computer as eight consecutive memory locations with a user selectable base address. This memory-mapped format allows unlimited D/A channel expansion by using multiple ST-703's, each with a different base address.

The ST-703 is pin compatible with the ST-724, SBC-724, and ST-728 analog output boards. The ST-703 may be used with both 8- and 16-bit microprocessors. The BHEN/line on the MULTIBUS sets the ST-703's address decoders and data latches for compatibility with 8- or 16-bit computers. The ST-703 also supports 24-bit MULTIBUS addressing capability and is downward compatible with 16- or 20-bit systems.

The most unique feature of the ST-703 is its 300 V channel-to-channel and channel-to-bus isolation. Applications include situations where a low-level analog signal must be superimposed on a high voltage, such as testing of power supplies, isolation amplifiers, et cetera. The ST-703 is also useful in applications where actuator failure could cause computer errors or destruction from line voltages being applied to the MULTIBUS. Isolation is accomplished through a combination of optoisolators for digital signals, and transformer isolation for power distribution. An onboard dc-to-dc converter provides four individually isolated supplies for the D/A converters.

The systems manual shipped with each board provides installation instructions, theory of operation, and engineering drawings.

GENERAL DESCRIPTION

Data inputs to the ST-703 are from the host computer's bus. Input coding may be straight binary, offset binary, or 2's complement, and is selectable on the board.

The MULTIBUS BHEN/line is used to set the ST-703's address and data coding for compatibility with 8- or 16-bit CPU's. In the eight-bit mode, the 12 bits of data required for the D/A converters are acquired in two bytes. The lower byte contains the four lower data bits, and is loaded into a storage register for each D/A channel on the ST-703. The next data byte contains the eight higher bits. Upon conversion, the eight MSB's and the four stored LSB's are loaded simultaneously into the DAC. In the 16-bit mode, all 12 data bits are transferred in a single word to the DAC data register. The register outputs are optically isolated and transferred to the D/A converter.

Each channel uses a DATEL model DAC-7541, a 12-bit monolithic device which offers linearity of ± .02% of full-scale range. The converter output is monotonic, having a differential nonlinearity of ± .02% FSR maximum. Offset error on each channel is preadjusted to zero. Trim positions on the board permit recalibration of zero (or offset) and gain settings. Two-speed versions of the board provide settling times of 5 μSec. and 30 μSec. respectively. Zero tempco is ± 2 ppm of FSR/degree Celsius and gain tempco is within ± 10 ppm of FSR/degree Celsius.

The output of each isolated DAC is fed to its own I-to-V conversion amplifier. A total of four voltage output ranges may be jumper selected by the user: 0 to +5V, 0 to +10V, ±5V, and ± 10V. In addition, a V-to-I converter circuit is provided for each D/A output channel. A 4 to 20 mA output, usable with an output load from 0 to 500 Ohms, is also jumper selectable.

The ST-703 contains a power-on reset circuit that allows each D/A output to be set to 0.000V at power-on time regardless of the input coding and output range configuration.

The current output requires an external excitation source, a +18V to +30V dc regulated supply capable of 25 mA per D/A channel. Voltage and current ranges on the ST-703 are selected individually for each channel. This allows a mix of voltage or current outputs on a single board.

The ST-703 is a memory-mapped peripheral occupying eight consecutive locations in the computer's address space. The board's base address is factory-set at 00FF10 Hex. However, a user may relocate the board address anywhere up to FFFFF8 on 8-byte boundaries using DIP switches on the board.

To make the ST-703 compatible with different speed CPU's and memory systems, a Transfer Acknowledge Delay (XACK/ Delay) is provided, permitting eight selectable delays from 0 to 700 nSec. in 100 nSec. increments.

The ST-703 is fully bus-, card cage-, and software-compatible with the MULTIBUS and with Intel RMX software. The board is 12.0 inches wide × 6.75 inches deep × 0.54 inch high (305 × 172 × 14 mm). Multiple ST-703 boards may be mounted in adjacent card slots when used with a standard .60 inch spacing Intel card cage.

The ST-703 draws all its power from the MULTIBUS +5V and +12V lines. An on-board dc-to-dc converter provides four isolated ±15V supplies to drive the analog output circuits.

The ST-703 weighs approximately 12 ounces (0,341 kilograms). It can operate over a temperature range of 0 to +55 degrees Celsius with relative humidity from 10 to 90% (non-condensing), and from 0 to 15,000 feet (0 to 4,600 m) in altitude.

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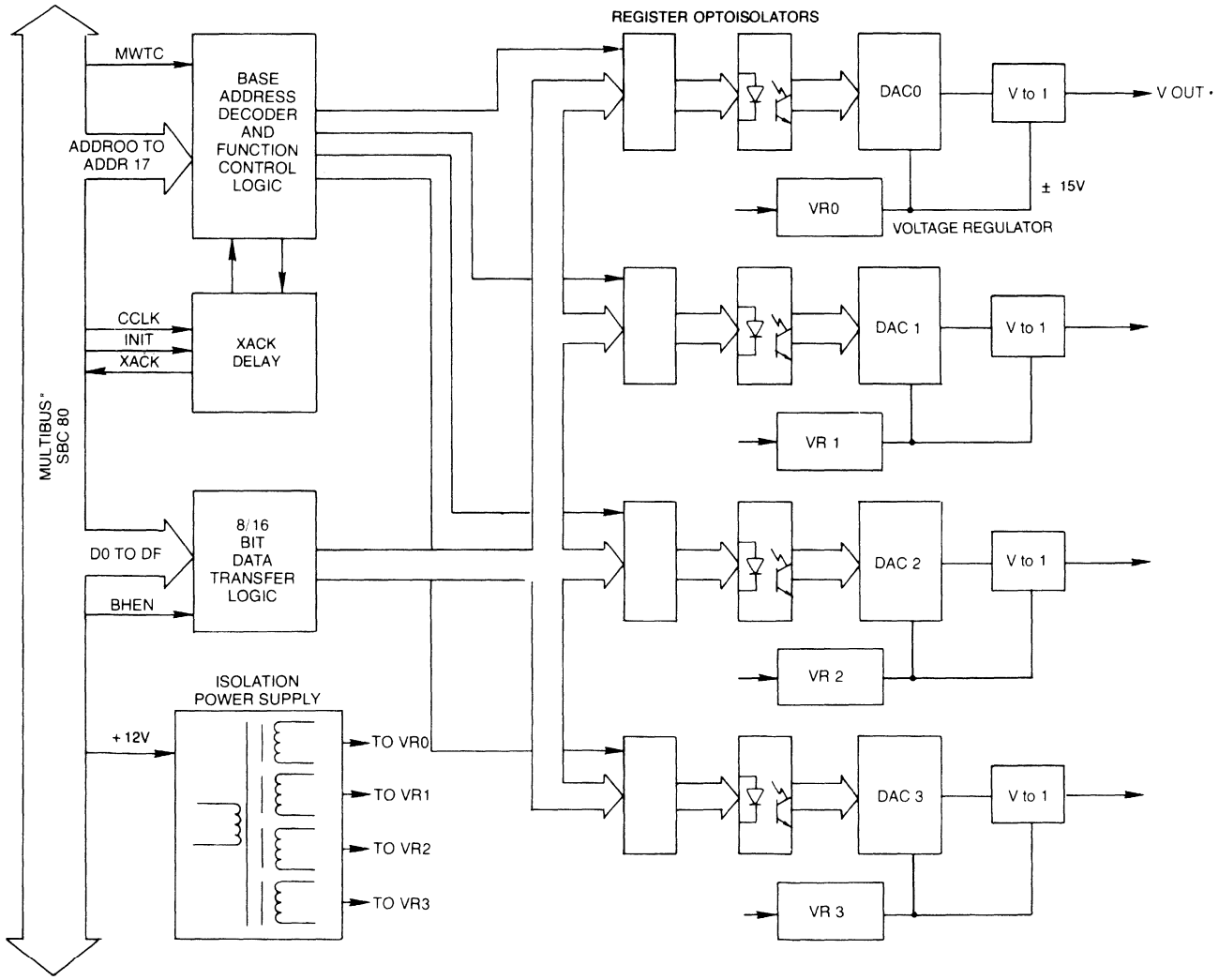
ST-703
BLOCK DIAGRAM



FUNCTIONAL SPECIFICATIONS

(typical at 25°C unless otherwise noted) — use generic.

D/A ANALOG OUTPUT

Number of Channels	4 D/A channels
Channel Expansion	Indefinite channel expansion using separate ST-703 boards at different base addresses; limited by available card slots and supply current
Full-Scale Output Ranges *	±10V (standard), ±5V, 0 to +5V, 0 to +10V, 4 to 20 mA — Individually selectable per channel
Digital Input Coding	Straight Binary, Offset Binary (standard), 2's Complement — Selectable per channel
Output Impedance	50 Milliohms
Output Current (Voltage Output)	Maximum ±5 mA @ ±10V short-circuit-proof to ground.
Current Loop Excitation Voltage	Maximum +10V to +30V, regulated, user supplied, 25 mA dc maximum channel.
Isolation Voltage (continuous)	300V RMS channel-to-channel and channel-to-bus

*NOTE: Outputs are short circuit protected.

ADDRESSING

Reserves a block of eight consecutive memory locations. Base address may be located on an eight byte boundary in the 24-bit CPU address space, provided the least significant byte equals 0 or 8 H.

PERFORMANCE

Accuracy at +25°C	±0.05% of FSR, ±1 LSB (includes noise and nonlinearity).
Differential Nonlinearity	±0.5 LSB, 0 to +55°C
Zero Temperature Drift (Unipolar Output)	Within ±5 ppm of FSR/°C
Offset Temperature Drift (Bipolar Output)	Within ±10 ppm of FSR/°C
Gain Temperature Drift	Within ±20 ppm of FSR/°C
Settling Time	
ST-703B	6 μSec. to 0.5 LSB of final value
ST-703A	30 μSec. to 0.5 LSB of final value
Slew Rate	8 V/μSec.

PHYSICAL

Outline Dimensions	12.00 inches wide x 6.75 inches deep x 0.54 inch high 304,8 wide x 171,5 deep x 13,7 high mm
Weight	12 ounces (0.34 kilograms)
Operating Temperature Range	−25 to +85°C
Storage Temperature Range	
Relative Humidity	10% to 90% non-condensing
Altitude	0 to 15,000 feet (4,600 M)

POWER CONSUMPTION

+5V @ 1 A
+12V @ 450 mA

GENERAL

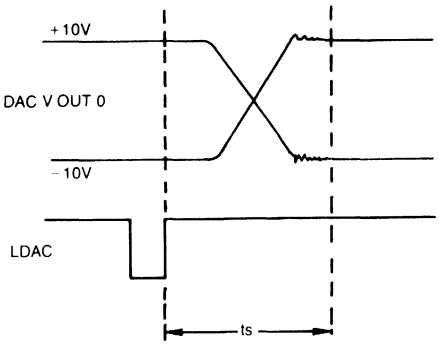
Bus Compatibility	Pin-for-pin, card guide, and program compatible with MULTIBUS (IEEE 796) and SBC series microcomputers.
CPU Compatibility	8- or 16-bit CPU compatible

ORDERING GUIDE

Model ST-703A	Isolated 4 Channel D/A board, 30 μsec. settling time
Model ST-703B*	Isolated 4 Channel board, 5 μsec. settling time

*Note: ST-703B should be selected for applications requiring low transient energy such as amplifier inputs.

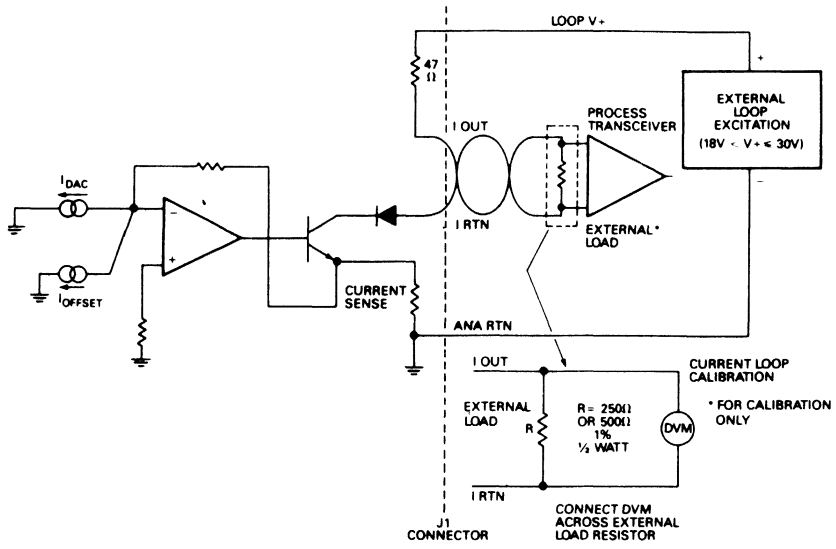
SETTLING TIME



ts: settling time = optoisolator delay + slew time + settling to ±½ LSB final voltage value

Full-scale output ranges*

TYPICAL CURRENT LOOP CIRCUIT



ST-703 USER'S CIRCUIT

DATA FORMAT

The ST-703 is a memory-mapped peripheral and appears to the CPU as a group of eight consecutive memory locations. Two locations are assigned to each D/A channel. The ST-703 requires 12 bits of digital data from the CPU for a single D/A conversion. The following chart shows how 8- and 16-bit CPU's format this data.

The ST-703 board automatically changes to a 16-bit format when the BHEN/line on the MULTIBUS goes to zero volts (pin 27 of the connector P1). Consequently, a high input on BHEN/ sets the ST-703 for the 8-bit format.

D15								SINGLE WORD (16-BIT CPU)							D0
HIGH BYTE (8-BIT CPU)								LOW BYTE (8-BIT CPU)							
D7							D0	D7							D0
DAC BIT 1 (MSB)	DAC BIT 2	DAC BIT 3	DAC BIT 4	DAC BIT 5	DAC BIT 6	DAC BIT 7	DAC BIT 8	DAC BIT 9	DAC BIT 10	DAC BIT 11	DAC BIT 12 (LSB)	X	X	X	X

X = Don't care

REGISTERS

Note that 8-bit CPU's must transfer the 12 data bits in two bytes. The low byte contains the four least-significant data bits which are stored in a register on the ST-703. The high byte contains the eight most-significant data bits. When the high byte is transferred, all 12 data bits are loaded into the DAC holding register and the D/A output is updated. Data transfer with a 16-bit CPU is done with a single word transfer; all 12 bits are simultaneously updated. Selection of 8- or 16-bit transfers is accomplished automatically, depending on the state of the MULTIBUS BHEN/line. The following chart details the memory address assignments of the ST-703 board. Note that when the ST-703 is used with a 16-bit CPU, data transfer must be to an even-numbered memory location.

ST-703 REGISTER ASSIGNMENTS

MEMORY ADDRESS (8-BIT CPU)	REGISTER ASSIGNMENT	MEMORY ADDRESS (16-BIT CPU)
BASE + 0	DAC 0 LSB Byte	BASE + 0
BASE + 1	DAC 0 MSB Byte	
BASE + 2	DAC 1 LSB Byte	BASE + 2
BASE + 3	DAC 1 MSB Byte	
BASE + 4	DAC 2 LSB Byte	BASE + 4
BASE + 5	DAC 2 MSB Byte	
BASE + 6	DAC 3 LSB Byte	BASE + 6
BASE + 7	DAC 3 MSB Byte	

BASE ADDRESS SELECTION

The ST-703 is a memory-mapped peripheral that occupies eight consecutive memory locations in the computer address space. The full 24-bit MULTIBUS addressing is supported, although the board may be used with CPU's that provide 16- or 20-bit addresses. The base address is selected by a combination of jumpers and DIP switches on the PC board. The board is factory-configured for 16-bit addressing and with a base address of 00FF10 hexidecimal.

24-, 20-, 16-BIT ADDRESS SELECT

Referring to the table below, remove or install the programming jumpers for the correct number of address select bits used in the system where the ST-703 is to be installed.

JUMPER	24 BIT	20 BIT	16 BIT
E103-E104	IN	OUT	OUT
E105-E106	IN	OUT	OUT
E107-E108	IN	OUT	OUT
E109-E110	IN	OUT	OUT
E111-E112	IN	IN	OUT
E 97-E 98	IN	IN	OUT
E 99-E100	IN	IN	OUT
E101-E102	IN	IN	OUT

BASE ADDRESS SELECTION

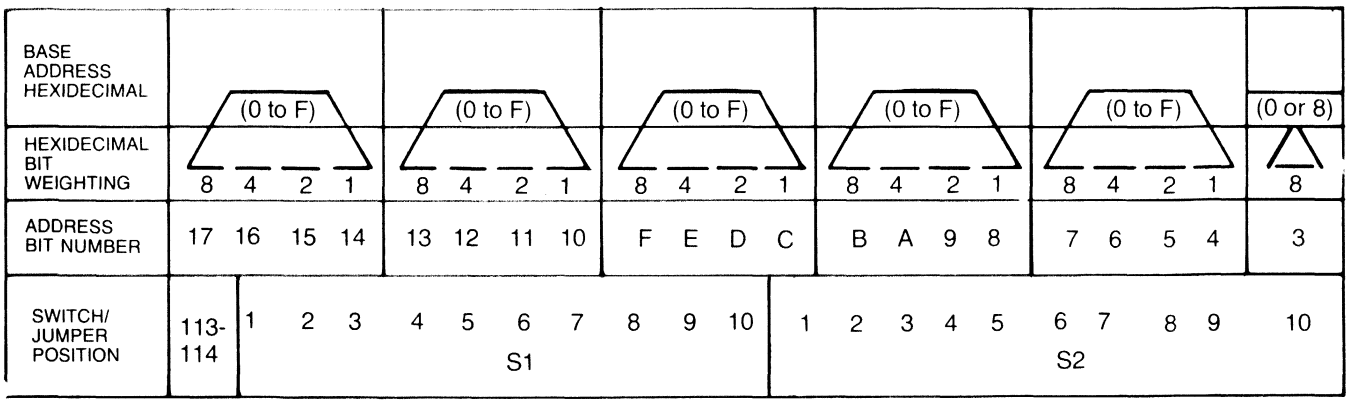
(1. Select a base address, in hexidecimal, and write it in Base Address, Hex.

(2. Convert the hexidecimal code to binary by writing 1's and 0's in the appropriate boxes (opposite Hex Bit Weighting).

(3. Set the base address desired on DIP switches S1 and S2. A closed switch (ON) corresponds to a 1 on the corresponding address line. An open (OFF) switch corresponds to a 0. Unused high order address switches must be left in the open (OFF) position. For example, if the CPU provides only 16 address lines, the address switches corresponding to ADR10 through ADR17 must be OFF.

1. To select a base address in hexidecimal use the following chart for changing configurations.

BASE ADDRESS SELECTION



TRANSFER ACKNOWLEDGE (XACK) DELAY SELECTOR

The ST-703 generates a Transfer Acknowledge (XACK) signal in response to memory/write commands from the MULTIBUS. It is sometimes desirable to delay this signal in order to match the signal to the CPU timing. A jumper selectable Transfer Acknowledge Delay, ranging from 100 to 800 nSec., is available in the ST-703. It should be noted that the XACK/delay is generated from the MULTIBUS CCLK/signal which is assumed to have a period of 100 nSec. Also, since this signal is asynchronous, the actual delay can only be set within a tolerance of one clock period, or 100 nSec. The jumper selections to configure the XACK/delay is as follows:

DELAY (nSec.) (standard)	JUMPER
100	E85 - E86
200	E87 - E88
300	E89 - E90
400	E93 - E94
500	E95 - E96
600	E91 - E92
700	E83 - E84
800	E81 - E82

Install only one jumper. The standard jumper from E85-E86 is connected in etch on the printed circuit board and must be cut if this jumper is changed.

INPUT CODING/POWER-ON RESET JUMPERS

The ST-703 may be configured to allow a choice of input coding formats. These are straight or offset binary, or 2's complement formats. In many applications it is desirable for the D/A converters to output a voltage of 0.000 Volts at power-on time. Jumpers are provided to accomplish this and depend on the range and input coding selected.

Jumpering is as follows:

INPUT CODING/POWER-ON RESET JUMPERS

INPUT CODING	DAC 0	DAC 1	DAC 2	DAC 3
Unipolar, Offset Binary	E61-E62 E58-E59	E66-E67 E63-E64	E73-E74 E70-E71	E78-E79 E75-E76
Bipolar, Offset Binary (Standard)	E61-E62 E57-E58	E66-E67 E64-E65	E73-E74 E69-E70	E78-E79 E76-E77
Unipolar, 2's Complement	E60-E61 E57-E58	E67-E68 E64-E65	E72-E73 E69-E70	E79-E80 E76-E77
Bipolar, 2's Complement	E60-E61 E58-E59	E67-E68 E63-E64	E72-E73 E70-E71	E79-E80 E75-E76

OUTPUT RANGE SELECTION

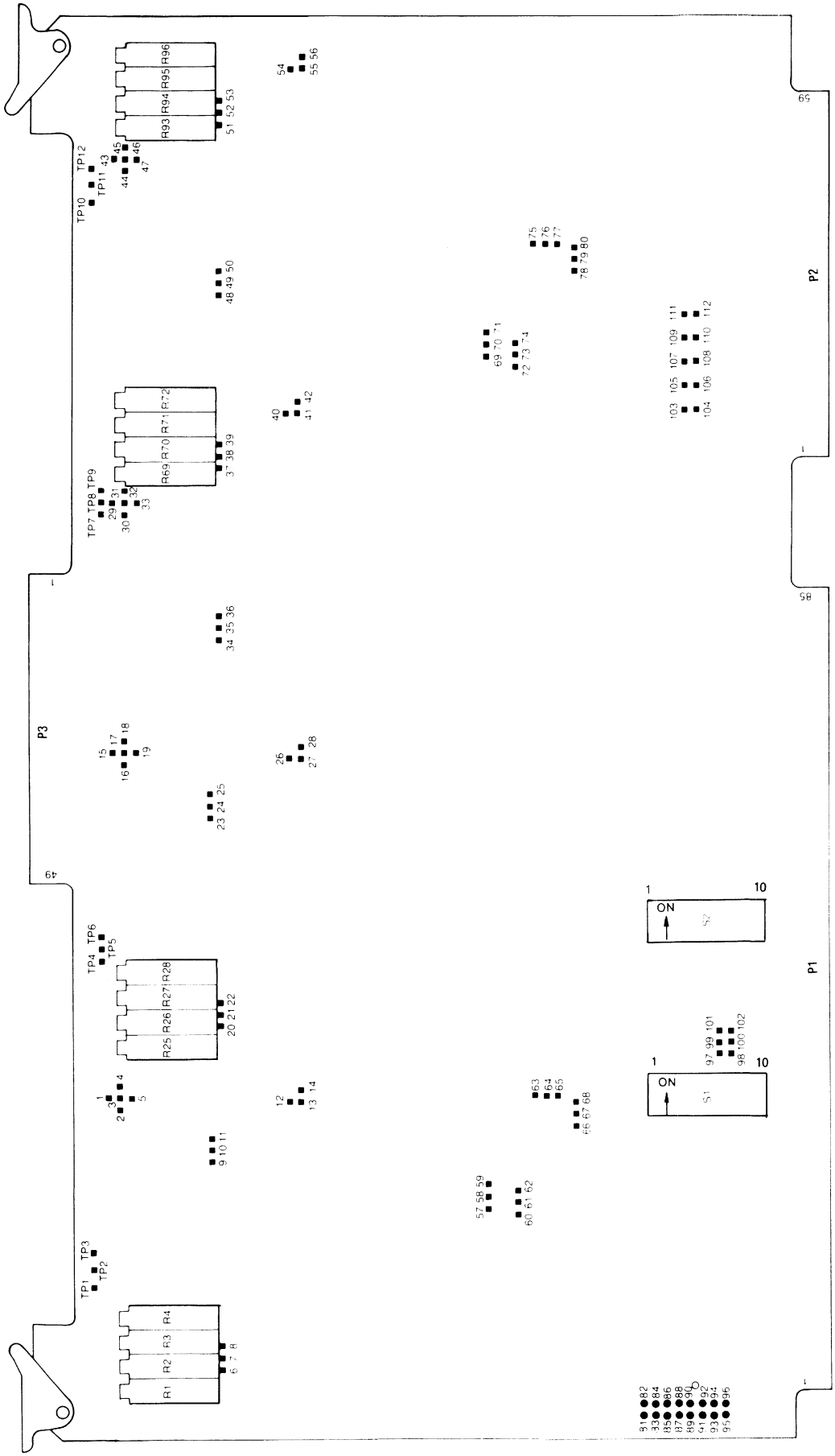
The output range of each D/A converter may be individually selected to provide a choice of four voltage output ranges or a single current loop range. The jumper-selected ranges may be set according to the following chart.

The ST-703 board is normally shipped with jumpers set for the ± 10V output, and an offset binary output coding. Whenever there is a change in output range on a given channel, that channel should be recalibrated.

OUTPUT RANGE JUMPERS

RANGE	DAC 0	DAC 1	DAC 2	DAC 3
0 to +5V	E9-E10 E1-E3	E23-E24 E15-E17	E34-E35 E29-E31	E48-E49 E43-E45
0 to +10V	E9-E10 E3-E5	E23-E24 E17-E19	E34-E35 E31-E33	E48-E49 E45-E47
+/−5V	E10-E11 E6-E7 E3-E5	E24-E25 E20-E21 E17-E19	E35-E36 E37-E38 E31-E33	E49-E50 E51-E52 E45-E47
+/−10V (Standard)	E10-E11 E7-E8 E3-E4	E24-E25 E21-E22 E17-E18	E35-E36 E38-E39 E31-E32	E49-E50 E52-E53 E45-E46
4 - 20 mA	E9-E10 E7-8 E2-E3	E23-E24 E21-E22 E16-E17	E34-E35 E38-E39 E30-E31	E48-E49 E52-E53 E44-E45

ST-703
BOARD LAYOUT



OPTOISOLATOR SPEED CONFIGURATION

The ST-703 is available with a choice of two setting time options. Since/because the DAC data lines are optically coupled, the DAC settling time is dependent on the switching times of the optoisolators used. A jumper is provided to select the settling time and is dependent on the type of optoisolator installed on the board.

SETTLING TIME JUMPER

MODEL	DAC 0	DAC 1	DAC 2	DAC 3
ST-703A	E12-E13	E26-E27	E40-E41	E54-E55
ST-703B	E13-E14	E27-E28	E41-E42	E55-E56

NOTE: The settling time jumper is programmed per the model number. It should not be changed to avoid permanent damage to the optoisolators.

CONNECTORS

The ST-703 board contains three connectors: P1 and P2 are the MULTIBUS connectors, and P3 is the Analog Output connector.

The P2 MULTIBUS connector is used only when a system controller's address is 24 bits. The pin assignment for the four (extended) address lines on P2 are shown in Table 1.

P3 is the Analog Output connector, which is described in Table 2. For current loop connection, refer to the current loop circuit.

Table 1. Multibus Connector (P2)

PIN	SIGNAL	FUNCTIONAL DESCRIPTION
55	ADR 16	
56	ADR 17	4 address line inputs
57	ADR 14	for 24 bit address controllers.
58	ADR 15	

Table 2. Analog Output Connector (P3)

PIN	(COMPONENT SIDE) FUNCTION	PIN	FUNCTION
	Pins 1 through 22 are no connection		
23	Analog Ground D/A CH 3	24	DAC V OUT CH 3
25	LOOP I RTN D/A CH 3	26	LOOP I IOUT CH 3
27	Analog Ground D/A CH 3	28	LOOP V EXC CH 3
29	Analog Ground D/A CH 2	30	DAC V OUT CH 2
31	LOOP I RTN D/A CH 2	32	LOOP I OUT CH 2
33	Analog Ground D/A CH 2	34	LOOP V EXC CH 2
35	Analog Ground D/A CH 1	36	DAC V OUT CH 1
37	LOOP I RTN D/A CH 1	38	LOOP I OUT CH 1
39	Analog Ground D/A CH 1	40	LOOP V EXC CH 1
41	Analog Ground D/A CH 0	42	DAC V OUT CH 0
43	LOOP I RTN D/A CH 0	44	LOOP I OUT CH 0
45	Analog Ground D/A CH 0	46	LOOP V EXC CH 0
47		48	
49		50	

NOTE: The Analog Ground lines for the D/A channels are not connected to each other or to the MULTIBUS ground.

CALIBRATION

The ST-703 board is calibrated for a voltage output range of ± 10V and Offset Binary coding. Calibration is required if the output range is changed for any of the D/A converters. A 4½ digit digital voltmeter is required. To calibrate the ST-703, perform the following steps in order.

1. Use the following table (specifications) to connect the digital voltmeter (DVM) to the test point, corresponding to the DAC to be calibrated.

(FULL-SCALE)
+9.9800 V REFERENCE ADJUSTMENT
TEST POINTS

	DAC 0	DAC 1	DAC 2	DAC 3
DVM + INPUT	TP1	TP4	TP7	TP10
DVM – INPUT	TP3	TP6	TP9	TP12
POT	R1	R25	R69	R93

Adjust the potentiometer for a reading of +9.9800 volts.

2. Connect the digital voltmeter (DVM) to the test point in the following table, corresponding to the DAC to be calibrated.

NEGATIVE REFERENCE ADJUSTMENT
TEST POINTS

	DAC 0	DAC 1	DAC 2	DAC 3
DVM + INPUT	TP2	TP5	TP8	TP11
DVM – INPUT	TP3	TP6	TP9	TP12
POT	R2	R26	R70	R94

Adjust the potentiometer for a reading of –2.500 volts if the DAC is to be configured for the ±5 Volt range. Otherwise, adjust the pot for a reading of –3.333 Volts.

3. Monitor the D/A output to be calibrated with the DVM. If calibrating for 4-20 mA output range, use a 250 Ohm .1% loop resistor to measure the voltage drop across the resistor.

Use the Diagnostic Test Program Calibration Test to enter the –full-scale hexidecimal data for the D/A channel under test. This data would be 0000 hexidecimal for binary coding, or 8,000 hexidecimal for 2's complement coding. Adjust the proper Zero (Offset) pot for the correct reading, as shown below.

ZERO OR OFFSET ADJUSTMENT POTENTIOMETERS

CHANNEL	POT
DAC 0	R3
DAC 1	R27
DAC 2	R71
DAC 3	R95

DAC – FULL-SCALE READINGS

RANGE	READING
0 to +5 V	0.0000 V
0 to +10 V	0.0000 V
±5V	– 5.0000 V
±10V	–10.0000 V
4 - 20 mA	1.0000 V

4. Monitor the D/A output to be calibrated with the DVM. Use the Diagnostic Test Program Calibration Test to enter the + full-scale hexidecimal data for the D/A channel under test. This data would be FFFF hexidecimal for binary coding, or 7FFF hexidecimal for 2's complement coding. Adjust the proper GAIN pot for the correct reading, as shown below.

GAIN ADJUSTMENT POTENTIOMETERS

CHANNEL	POT
DAC 0	R4
DAC 1	R28
DAC 2	R72
DAC 3	R96

DAC + FULL-SCALE READINGS

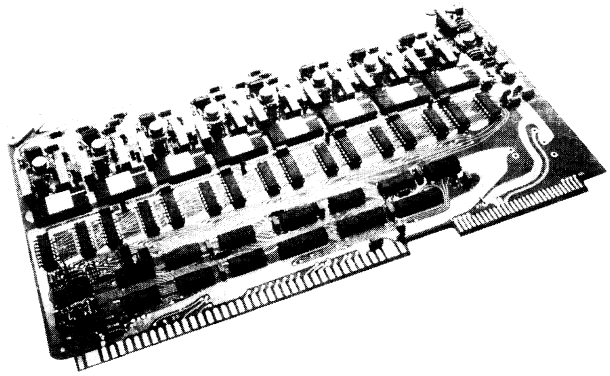
RANGE	READING
0 to +5 V	+4.9988 V
0 to +10 V	+9.9976 V
±5V	+4.9976 V
±10 V	+9.9951 V
4 - 20 mA	+4.9990 V

SineTrac™ D/A and Current Loop Boards for MULTIBUS® Microcomputers

SineTrac™ ST-716

FEATURES

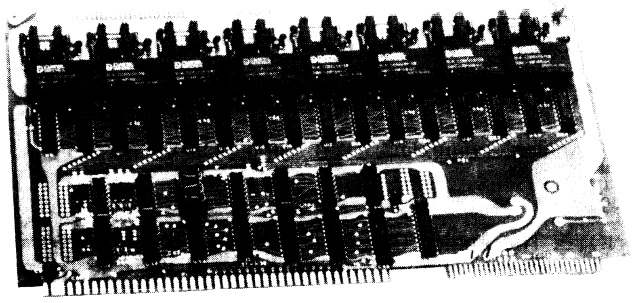
- **4 or 8 D/A Channels, 16-bit resolution**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Accurate to 0.005% of full-scale reading**
- **Complete hardware and software compatibility with MULTIBUS and iSBC-Series microcomputers**
- **20-Bit addressing**
- **Memory-mapped, with User-Selectable Base Address**
- **Three user-selectable output ranges available: ±5V dc, and 0 ⟶ +10V dc, ±10V dc**
- **Selectable Transfer Acknowledge Delay (XACK/); ensures compatibility with different memory speeds**



SineTrac™ ST-728

FEATURES

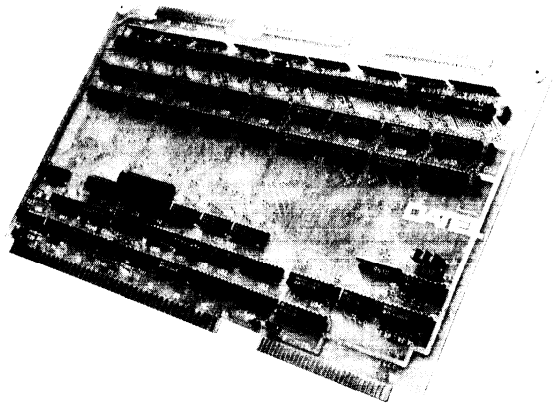
- **4 or 8 D/A channels, 12-bit resolution**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Accurate to .05% of full-scale reading**
- **Complete hardware and software compatibility with MULTIBUS and iSBC-Series microcomputers**
- **Memory-mapped, with user-selectable Base Address, 16-, 20- or 24-bit addressing**
- **Three user-selectable input data codes: Straight Binary, Offset Binary, or Two's Complement**
- **Five user-selectable output ranges available: ±5V dc, ±10V dc, 0 ⟶ +10V dc, 0 ⟶ +10V dc, and 4-20 mA current loop, individually selected for each channel**
- **Selectable Transfer Acknowledge Delay (XACK/); ensures compatibility with different memory speeds**



ST-519
MULTIBUS 72-Line Digital I/O Board With Interrupt

FEATURES

- **72 Individually-programmable input/output lines**
- **IEEE 796 MULTIBUS Compatible**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Memory mapped, optional I/O map**
- **16-, 20- or 24- bit user-selectable base address**
- **Eight maskable interrupt lines**
- **Interfaces to pluggable modules for 2.5KV isolation**



DATEL expands its line of MULTIBUS compatible system boards with the ST-519. The ST-519 provides 72 individually-programmable lines for input or output (I/O). Also, an interrupt controller is provided to allow up to eight user-programmable interrupt lines. Like other DATEL MULTIBUS products, the ST-519 is fully hardware- and software-compatible with all MULTIBUS microcomputers. All necessary address decoders, logic controls, and data transceivers are incorporated on board.

DESCRIPTION

The DATEL ST-519 is a MULTIBUS-compatible system board providing 72 software programmable input/output (I/O) lines. These I/O lines are fully TTL compatible and each line can be individually programmed as either an input or an output.

The ST-519 may be used with both 8- and 16-bit microprocessors. The BHEN/line on the MULTIBUS sets the ST-519's address decoders and data latches for compatibility with 8- or 16-bit computers. The ST-519 also supports 24-bit MULTIBUS addressing capability, and is downward compatible with 16- or 20-bit address systems.

The ST-519 has an 8259A Programmable Interrupt Controller which provides vectoring information for eight user-definable interrupt levels. In normal slave operation, the Interrupt Request (IR) lines of the 8259A are hard-wired to an I/O line. When the I/O event occurs the 8259A generates an Interrupt (INT) which would go to one of the MULTIBUS vector interrupt lines INTØ thru INT7.

The 72 I/O lines are brought out on three 50-pin edge-card connectors: J1, J2, and J3. These edge-card connectors are fully compatible to the Gordos and OPTO 22 type pluggable modules systems that offer an input to output isolation of 2.5K VAC. A flat ribbon cable interconnects the DATEL ST-519 to other electronic module systems.

The ST-519 is a memory-mapped peripheral occupying 16 consecutive locations in the computer's address space. The board's base address is preset at ØØFFAØ hex. However, a user may relocate the board address anywhere up to FFFFFØ on 16-byte boundaries using DIP switches on the board.

In order to make the ST-519 compatible with different speed CPU and memory systems, a transfer acknowledge delay (XACK/DELAY) is provided. This permits 8 selectable delays from 100 to 800 nanoseconds.

The ST-519 is fully bus- and card-cage compatible with the MULTIBUS and IEEE 796. The board is 12.0"W x 6.75"D x 0.47"H (305 x 172 x 12 mm). When used with the standard MULTIBUS card cage, the ST-519 board may be installed adjacent to other boards.

The ST-519 draws all power from the MULTIBUS +5V dc power line. The ST-519 weighs approximately 12 ounces (0,341 kg). It can operate over a temperature range of 0 to +55 degrees Celcius with relative humidity from 10 to 90% (noncondensing), and from 0 to 15,000 feet (0 to 4,600 m) in altitude.

Compatible to Opto-22, PB-16, or PB-24 I/O panels or equivalent.

ORDERING GUIDE

MODEL	DESCRIPTION
ST-519	72 line digital I/O board with interrupt

FUNCTIONAL SPECIFICATIONS

CHANNELS

I/O number of channels..... 72 I/O Channels
Channel expansion.... Indefinite channel expansion using separate ST-519 boards at different base addresses; limited by available card slots and supply current

OUTPUT DRIVER

Output current sink (Vout = 0.6V)..... 24 mA (max.)
Output current source (Open collector 4.7KΩ from +5V)..... 1 mA (max.)

INPUT RECEIVER

High level input current (Vin = 2.7V).....100 µA (max.)
Low level input current (Vin = 0.4V).....-1.2 mA (max.)

ADDRESSING

Occupies a block of 16 consecutive memory (I/O) locations. Base address may be located on any 16 byte boundary in the 16-, 20- or 24-bit address space by two DIP switches.

PHYSICAL

Outline Dimensions... 12.00"W x 6.75"D x 0.50"H (max.)
304,8W x 171,5D x 12,7H mm
Weight..... 12 ounces (0.34 kg)
Operating Temperature Range..... 0 to +55°C
Storage Temperature Range..... -25 to +85°C
Relative Humidity..... 10% to 90% non-condensing
Altitude..... 0 to 15,000 feet (4,600 m)

POWER CONSUMPTION +5V dc ±5%

ST-519 (stand alone)..... 1.7 A typical
ST-519 + 72 I/O modules.....3.3 A typical

GENERAL

Bus Compatibility..... Pin-for-pin, card guide, and program compatible with MULTIBUS (IEEE 796) and SBC series microcomputers
CPU Compatibility.....8 or 16 bit compatible

DATA FORMAT

The ST-519 is a memory-mapped peripheral that appears to the system CPU as 16 bytes of consecutive memory. These registers can be accessed as 16 single bytes (8-bit CPU) or as 8 double bytes (16-bit CPU).

The ST-519 board automatically changes to a 16-bit format when the BHEN/line on the MULTIBUS pin 27 of connector P1 goes to zero volts. A high input on BHEN/, consequently, sets the board for an 8-bit format.

INTERRUPT

An 8259A Programmable Interrupt Controller provides onboard interrupt generation to the host's interrupt controller. This device generates interrupts on low-to-high transitions from user-selected digital inputs coming into the ST-519. Jumpers (pins 64 through 71) tie the selected digital input lines directly to the selected IR interrupt.

Jumper pins 64 through 71 have two different uses based upon the mode of operation. In one mode, the MULTIBUS interrupt priority level (INT 0-7) is jumper-selectable between pin 111 (INT) and the jumper pins for the priority levels as outlined below (pins 103, 104, 105 . . .). For this single-interrupt scheme, the user wires the interrupt source to an interrupt input pin (pins 64 through 71). Jumper pins 97 through 101, 109 and 110 are not used in this mode.

In the other mode, up to eight interrupt levels are defined using eight digital input bits to the ST-519. Each input has a jumper, pins 97 through 113 (excluding 111). Pins 64 through 71 are user-prioritized and connected (through buffers and jumpers) to the MULTIBUS INT 0-7 lines. This mode bypasses the 8259A and its interrupt vector address function. Use this mode when the host provides the necessary vectoring information for servicing the interrupt caused by the digital input.

8259A		MULTIBUS	
Line Name	ST-519 Jumper Pin#	Line Name	ST-519 Jumper Pin#
INT	111	INT0	112
IR0	67	INT1	113
IR1	68	INT2	107
IR2	66	INT3	108
IR3	71	INT4	105
IR4	65	INT5	106
IR5	70	INT6	103
IR6	64	INT7	104
IR7	69		

CONNECTORS

The ST-519 board contains five connectors: P1 and P2 are the MULTIBUS connectors, and J1, J2, and J3 are the digital I/O connectors.

The P2 MULTIBUS connector is used only when a system controller's address capability is 24 bits. The pin assignment for the four extended address lines on P2 are shown in Table 1.

The digital I/O lines use connectors J1, J2, and J3; Table 2 describes these connections.

Table 1. MULTIBUS Connector P2

PIN	SIGNAL	Functional Description
55	ADR 16	
56	ADR 17	4 address line inputs for 24
57	ADR 14	bit address controllers
58	ADR 15	

Table 2. I/O Connector

Connector Pin Number	J1 Register Addr	J1 Bit	J2 Register Addr	J2 Bit	J3 Register Addr	J3 Bit	I/O Module	Connector Pin Number	J1 Register Addr	J1 Bit	J2 Register Addr	J2 Bit	J3 Register Addr	J3 Bit	I/O Module
2	2	7	5	7	8	7	23	26	1	3	4	3	7	3	11
4	2	6	5	6	8	6	22	28	1	2	4	2	7	2	10
6	2	5	5	5	8	5	21	30	1	1	4	1	7	1	9
8	2	4	5	4	8	4	20	32	1	0	4	0	7	0	8
10	2	3	5	3	8	3	19	34	0	7	3	7	6	7	7
12	2	2	5	2	8	2	18	36	0	6	3	6	6	6	6
14	2	1	5	1	8	1	17	38	0	5	3	5	6	5	5
16	2	0	5	0	8	0	16	40	0	4	3	4	6	4	4
18	1	7	4	7	7	7	15	42	0	3	3	3	6	3	3
20	1	6	4	6	7	6	14	44	0	2	3	2	6	2	2
22	1	5	4	5	7	5	13	46	0	1	3	1	6	1	1
24	1	4	4	4	7	4	12	48	0	0	3	0	6	0	0

1–49: All odd number pins are tied to ground.

REGISTER

The following chart details the memory address assignments of the 16 memory locations the ST-519 occupies. Please note that when the ST-519 is used with 16-bit CPU's, every other (even-numbered) address location is used.

ST-519 Register Assignments

8 BIT CPU ADDRESS	FUNCTION	REGISTER	COMMENTS	ADDRESS (16 BIT CPU)
BASE + 0	WRITE	WRITE OUTPUT 0–7	REG 0 J1	
BASE + 0	READ	READ INPUT 0–7		BASE + 0
BASE + 1	WRITE	WRITE OUTPUT 8–15	REG 1 J1	
BASE + 1	READ	READ INPUT 8–15		
BASE + 2	WRITE	WRITE OUTPUT 16–23	REG 2 J1	
BASE + 2	READ	READ INPUT 16–23		BASE + 2
BASE + 3	WRITE	WRITE OUTPUT 24–31	REG 3 J2	
BASE + 3	READ	READ INPUT 24–31		
BASE + 4	WRITE	WRITE OUTPUT 32–39	REG 4 J2	
BASE + 4	READ	READ INPUT 32–39		BASE + 4
BASE + 5	WRITE	WRITE OUTPUT 40–47	REG 5 J2	
BASE + 5	READ	READ INPUT 40–47		
BASE + 6	WRITE	WRITE OUTPUT 48–55	REG 6 J3	
BASE + 6	READ	READ INPUT 48–55		BASE + 6
BASE + 7	WRITE	WRITE OUTPUT 56–63	REG 7 J3	
BASE + 7	READ	READ INPUT 56–63		
BASE + 8	WRITE	WRITE OUTPUT 64–71	REG 8 J3	
BASE + 8	READ	READ INPUT 64–71		BASE + 8
BASE + 9	—	NOT USED		
BASE + A	WRITE	CLEAR OUTPUT REG 0–7	CLR REG 0	
BASE + A	READ	READ CLEAR REG		BASE + A
BASE + B	WRITE	CLEAR OUTPUT REG 8	CLR REG 1	
BASE + B	READ	READ CLEAR REG		
BASE + C	WRITE	CONTROL REG 1, 8259A	8259A	
BASE + C	READ	STATUS REG 1, 8259A	INTERRUPT	BASE + C
BASE + D	—	—	CONTROLLER	
BASE + D	—	—	Refer to INTEL data sheet	
BASE + E	WRITE	CONTROL REG 2, 8259A		
BASE + E	READ	STATUS REG 2, 8259A		BASE + E
BASE + F	—	—		
BASE + F	—	—		

CLEAR REGISTERS

The clear registers are used to clear (reset) the output registers to all 0's. On power-up or system reset, the clear register bits reset all output registers which disables all output lines. Only after the clear register bits have been set to 1's will the output (write) function be enabled.

The clear registers format is shown. Refer to I/O line section for programming of input/output registers.

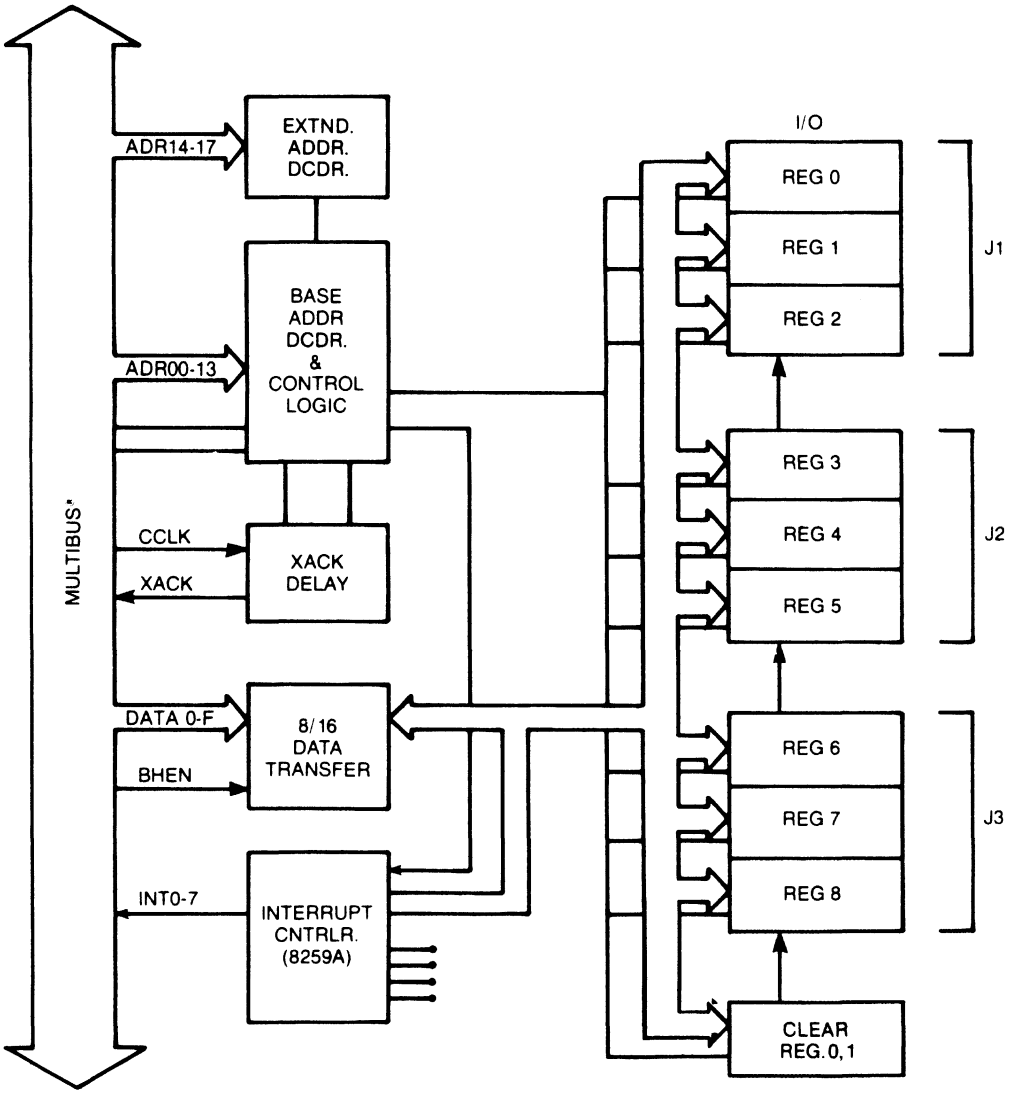
CLEAR REGISTER FORMAT

							CLR REG (16 BIT CPU)								
DF															D0
							CLR REG 1							CLR REG 0	
D7							(8 BIT CPU)			D0	D7			(8 BIT CPU)	D0
X	X	X	X	X	X	X	8	7	6	5	4	3	2	1	0
DON'T CARE							OUTPUT REGISTER CLEARED								

When a clear register bit is 0, the corresponding output register is cleared forcing output lines to logic high (1).

When a clear register bit is 1, the corresponding output register is enabled to be programmed.

ST-519 Block Diagram



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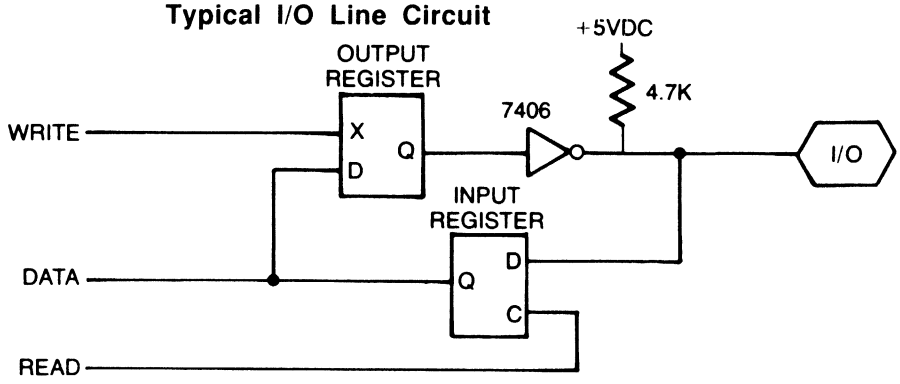
I/O LINE

All output lines are comprised of an output latch driving an inverting open collector output buffer. During a write cycle to an output register, the data latched will appear inverted at the edge card connector. If the status of an output line is read back thru the ST-519, the previously written data will appear inverted.

An I/O line which is to be used as an input must have its corresponding output line set to a zero. During a read cycle, data from an input line is the true logic level from the edge card connector.

Typical I/O Line Circuit



24 BIT ADDRESS SELECT

The ST-519 is factory configured for 16- or 20-bit addressing. A 24-bit adddress capability is selected by installing programming plugs and soldering a jumper as follows:

1. Cut and remove etch between 46–47.
2. Install wire jumper between 48–47, solder the jumper.
3. Install programming plugs at 75–83, 77–85, 79–87, and 81–89.

BASE ADDRESS SELECTION

The ST-519 is a memory-mapped peripheral that occupies 16 consecutive, byte-wide, memory locations in the computer address space. The base address decoding supports both 16- and 20-bit addressig with 24-bit address capability being optional. Base address selection is accomplished by setting DIP switches on the PC board.

1. Select a base address, in hex, between 000X (00000X) and FFFX (FFFFFX). Write the base address in the Base Address, Hex boxes.
2. Convert the hex code to binary by writing 1's and 0's in the Hex Bit Weighting boxes.
3. Set the desired base address on DIP switch S1 and S2 or the jumper area for extended address. A switch position ON or a wire jumper corresponds to a "1". An OFF switch position or a removed wire jumper corresponds to a "0". If the CPU provides only 16 address lines, the address switches corresponding to ADR10/ through ADR13/ must be left OFF.

BASE ADDRESS HEX	(0 to F)				(0 to F)				(0 to F)				(0 TO F)				(0 TO F)			
HEX BIT WEIGHTING	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
ADDRESS BIT #	17	16	15	14	13	12	11	10	F	E	D	C	B	A	9	8	7	6	5	4
SWITCH/ JUMPER POSITION	84-76	86-78	88-80	90-82	S1 1	S1 2	S1 3	S1 4	S1 5	S1 6	S1 7	S1 8	S2 1	S2 2	S2 3	S2 4	S2 5	S2 6	S2 7	S2 8

I/O SELECT

The ST-519 is factory configured as a memory-mapped peripheral. I/O addressing is an option that may be selected by soldering jumpers by:

1. Cutting and removing etch between 96–93 and 95–91.

2. Installing wire jumpers between 94–93 and 92–91; solder the jumpers.

INPUT PORT MODE SELECT

Each I/O line consists of an output latch driving a 7406 open collector output buffer, and an input device which can be jumper programmed as a transparent input buffer or as an input latch.

Each card edge connection (J1, J2, and J3) has a group of three ports with associated logic circuitry and jumpers to provide the end-user with the capability to latch one or more of the input ports on any given event. At each port group there is an inverter/ jumper network to select the polarity of the latching function.

The input ports are factory configured to appear as three-state transparent buffers. The latched input port option is selected by removing circuit-etch jumpers, and then soldering wire jumpers for the input port(s) to be changed. Refer to the Input Port Mode Select chart.

The level and the event that latches the ports must also be selected by the end-user. The port latch event is factory configured to be a positive level (logic level one). A negative level (logic level zero) option is selected by programming plug. The port latch event input must then be hardwired to the event (I/O line, Interrupt Required) that will control the latching of the input port(s).

Refer to the Input Port Mode select chart.

		INPUT PORT		PORT LATCH EVENT		
CONN.	REGISTER	TRANSPARENT (STANDARD)	LATCHED (OPTIONAL*)	POSITIVE (STANDARD)	NEGATIVE (OPTION)	INPUT
J1	REG 0 REG 1 REG 2	7-8 10-11 13-14	8-9 11-12 14-15	37-43	37-38	49
J2	REG 3 REG 4 REG 5	16-17 19-20 22-23	17-18 20-21 23-24	39-44	39-40	50
J3	REG 6 REG 7 REG 8	25-26 28-29 31-32	26-27 29-30 32-33	41-45	41-42	51

*To program to OPTION, first remove etch jumpers under standard and then install and solder option jumpers.

TRANSFER ACKNOWLEDGE (XACK) DELAY SELECTION

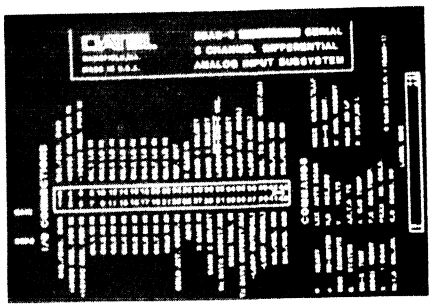
The ST-519 generates a transfer acknowledge (XACK/) signal in response to read or write commands from the MULTIBUS. It is sometimes desirable to delay this signal in order to match this signal to the CPU timing. A jumper selectable transfer acknowledge delay ranging from 100 to 800 nanoseconds is available on the ST-519. It should be noted that the XACK/ delay is generated from the MULTIBUS CCLK/ signal which is assumed to have a period of 100 nanoseconds. Also, since this signal is asynchronous, the actual delay can only be set within a tolerance of one clock period or 100 nanoseconds. The accuracy of the XACK/ delay is dependent on the period (T) of the CCLK signal generated by the host computer. The programming of XACK/ delay is in multiple increments of T, ranging from one to a maximum of eight, refer to XACK/ delay selection table below.

DELAY		JUMPERS
100 nsec.		52-53
200 nsec.	(Standard)	52-54
300 nsec.		52-55
400 nsec.		52-56
500 nsec.		52-57
600 nsec.		52-58
700 nsec.		52-59
800 nsec.		52-60

SDAS-8
Analog Input 8 Channel Differential Serial Microsystem

SDAS-8 FEATURES

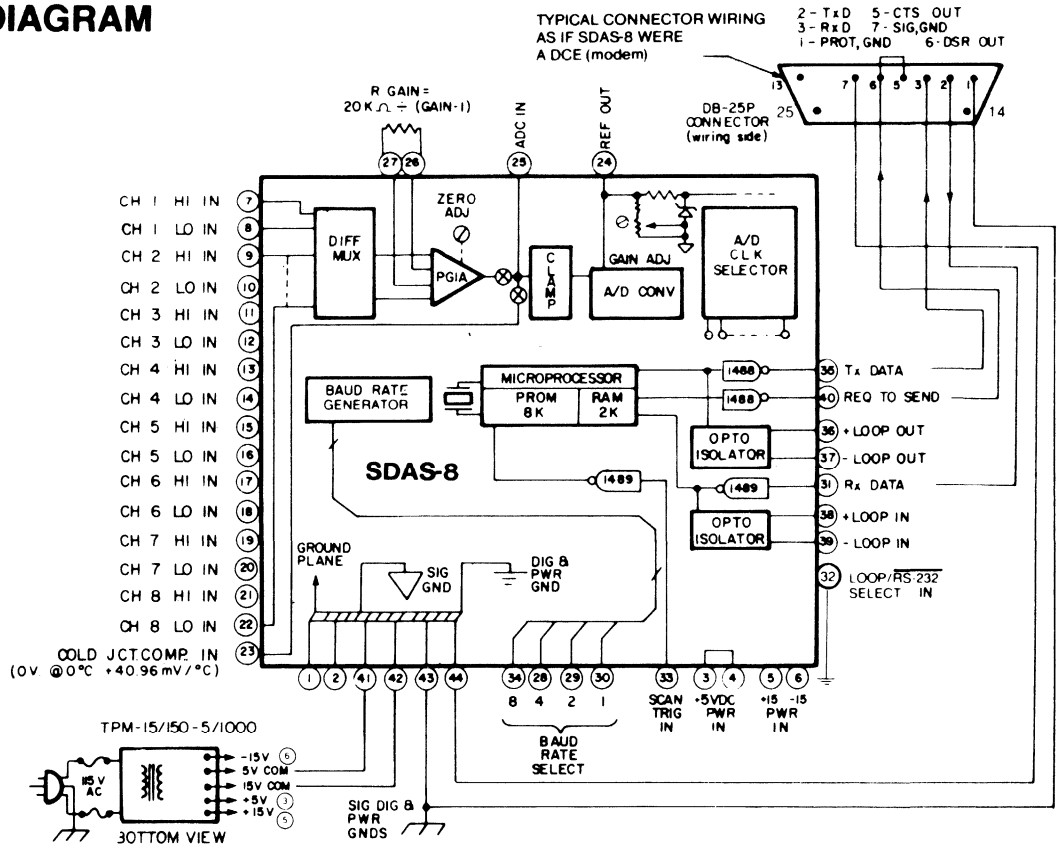
- 8 Differential Analog Input Channels, ±4.095Vdc full scale.
- Serial RS-232-C full duplex data link, 75-9600 baud.
- Simple ASCII commands.
- Direct thermocouple input (J, K, S, T) and linearization.
- Resistor-selected gain ×1 to ×200.
- Includes crystal time-of-day clock (23:59:59).
- Output is command-selected as ASCII hexadecimal or decimal, volts, °F or °C.
- A/D resolution is 12 bit binary and polarity (13 bits)
- Choice of 50 to 60 Hz normal mode AC rejection.
- Also includes optoisolated (2500Vpk) 20mA serial loop I/O
- 3 scan transmit start methods
  1. Local 10 μS TTL trigger input.
  2. Polled by host ASCII command.
  3. Auto-start using internal timer, 1 second to 17:59:59 hours intervals.
- 4″ × 6″ × 0.4″ steel-cased module, for direct PC-board mounting or standoffs.
- Uses regulated +5Vdc @ 500mA, ±15Vdc @ 50mA power.
- Easily interfaces to popular RS-232-C terminals, microcomputers and serial-port personal computers.
- May be positioned many hundreds of feet from host.
- Multidrop up to 4 stations (32 differential channels) using the 20mA serial I/O.
- Extensive editing, formatting and ident. header controls.



APPLICATIONS

- Simple A/D input to any RS-232-C terminal.
- Remote data logging to any host computer.
- Direct data acquisition mode with clock for any printer from local TTL trigger scan transmit.
- Diagnostic instruments, analytical systems, multichannel computer-controlled test equipment.

SIMPLIFIED BLOCK DIAGRAM



INTRODUCTION

Designed to simplify the connection of analog input signals to digital computers, the SDAS-8 is an 8-channel differential input A/D smart microsystem combined with a full-serial, full duplex terminal I/O port operated by an internal microprocessor. The serial port accepts input commands from the user's host computer or terminal and transmits ASCII analog data and status from dc or slowly varying transducer signals. The SDAS-8 is housed in a steel-cased modular package measuring only 4" × 6" × 0.4" for printed circuit board or standoff mounting. Using standard RS-232-C serial interfacing levels and simple ASCII commands, the SDAS-8 connects to all popular computers including personal computers with a programmable serial port.

The normal application for SDAS-8 is as a remote analog data input to a computer. The user's host computer would take the SDAS-8 data strings under program control and would process this data for arithmetic manipulation (peak detection, averaging, scaling and offset), display formatting (columnizing data with engineering unit labels), data storage to disk or tape or data retransmission.

SPECIAL FEATURES

SDAS-8 includes two onboard crystal-stabilized clocks, both of which are controlled and displayed with simple user commands. A settable 24-hour (23:59:59) time of day clock may be optionally tagged with each returned data scan transmission. A selectable independent interval timer causes automatic scan transmissions from 1 second to 17:59:59 hours intervals. Direct thermocouple inputs are available using the gain-selected, resistor-programmed instrumentation amplifier and a separate cold-junction compensation input channel. Under serial ASCII command, SDAS will directly linearize type J, K, T and S thermocouples with software correction for the local TC-to-copper cold junction EMF error using an external connector temperature sensor. Other ASCII commands produce direct data output in degrees Celsius or Fahrenheit from thermocouple inputs.

SDAS-8 includes both RS-232-C (non-isolated) and 20mA loop (isolated) serial ports. Using the loop ports, up to 4 SDAS-8 stations (32 Differential channels) may be multi-dropped in series on input and output loops (4 wires).

Individual channels may then be polled under host computer command many hundreds of feet away.

Requiring regulated +5V and ±15V dc power, SDAS-8 readily adapts to existing computers. Remote 2-wire data acquisition to any distance requires the addition of standard RS-232-C auto-dial, auto-answer telephone modems at both ends.

The standard SDAS-8 analog input range is ±4.095Vdc full scale at a gain of one. Analog signals are converted to a 12-bit binary representation plus polarity for bipolar signals, yielding a resolution of one part in 8192. For programming convenience, channel data is transmitted either as ASCII decimal or as ASCII hexadecimal under serial command. To simplify program number conversion, bit weighting in hex is 1 millivolt per count at gain = 1. All data is tagged with a hexadecimal checksum which may be compared for data link integrity.

The differential instrumentation amplifier is gain programmable with an external, user-supplied precision resistor for practical gains up to X200. For J and K thermocouples, SDAS-8 is calibrated for a gain of X80. S and T thermocouples require a gain of X160. The gain resistor is omitted for the gain-of-one ±4.095Vdc range.

The dual-slope, sign/magnitude A/D converter used in SDAS-8 continually overwrites a local random access semiconductor memory (RAM) buffer at 15 samples per second (12.5Hz for 50Hz NMR). Depending on baud rate, protocol overhead and formatting, per channel bandwidth is typically 1Hz.

A/D scan transmissions may be started by the remote host computer in polled mode or after host initialization of the SDAS-8 autostart timer. Scan starts may also occur using a local TTL start trigger input. In this mode, no host computer is needed. SDAS-8 will directly transmit to a serial input printer such as Datel's MPP-20 or APP-48 series.

A wealth of formatting controls are included for manual set-up, evaluation and calibration. Line length may be command-selected from 20 to 132 characters per line. Editing features include two types of rubout format, similar to micro-computer monitor programs. Line feed characters may be suppressed and filler NUL's may be command-selected for slow printers. Syntax errors which won't execute are echoed with a "#."

A status message indicates system state at any time. Half duplex operation may be invoked by suppressing the character echo and the string transmission can be throttled for host input buffer management using the XON/XOFF commands. A selectable (20 character) identification message may precede all data to tag the location, date, scale factors, etc. Line formatting prevents skewing or slicing of data for any one channel over two lines.

Careful selection of A/D integration periods offers rejection of 50 or 60Hz input noise.

SDAS-8 input/output connections are made through a dual-row right-angle connector whose mating pins may be PC board mounted or adapted to a flat cable header.

ST-705: A COMPLETE SDAS-8 SINGLE BOARD SUBSYSTEM

SDAS-8 is also available on the Model ST-705 single-board system which includes an AC power supply, screw-terminal analog input connections and a standard 25-pin RS-232-C DB-25P connector for direct plug-in to the user's terminal or computer. The ST-705 also includes the local thermocouple cold-junction compensation amplifier and connector temperature sensor. For local triggered scan starts, a TTL one-shot circuit accepts a switch input. Extra PC board pads are included for user-installed input voltage dividers (higher voltage ranges), current shunts (direct 4-20mA measurement, etc.) overvoltage protection clamp zeners or RC hash filters. Barrier screw terminals are installed to connect an AC line cord and pads are included for user-installed gain resistors.

The ST-705 is configured on a Multibus format PC board for mounting convenience in Multibus stand-alone card cages or in the user's host Multibus computer. The ST-705 may also be mounted in a separate chassis on standoffs. Although the ST-705 does not connect to the Multibus computer signals, pads are included to use +5V and ±15Vdc power from the host computer, thereby eliminating the ST-705 AC power supply. Using a combination of the transformer-isolated AC supply and the opto-isolated 20mA loop serial port, full isolation of the analog inputs is achieved on the ST-705.

SPECIFICATIONS

(Typical at +25°C, rated power unless otherwise noted)

ANALOG INPUT

Number of channels — 8 Differential plus single-ended CJC input*

*V_{CJC} IN = (Connector Temp. −0°C) × 40.96mV

Configuration — High impedance, non-isolated, voltage input, true balanced differential.

Full Scale Input Range — ±4.095 Volts dc (standard), gain = 1. The full scale input range may be reduced up to gains of X200 using an external user-supplied gain programming resistor.

Full Scale Temperature Ranges (using calibrated thermocouples and external cold junction compensation).

J Type	−165° C to +760°C
K Type	−165°C to +1232°C
S Type	0°C to +1768°C
T Type	−200°C to +400°C

Common Mode Voltage Range — ±11V max. referred to signal common (user's external input circuit must prevent exceeding CMV range).

Common Mode Rejection — 70 dB min., dc to 60 Hz, 1 kilohm unbalance, GAIN = 1

Input Overvoltage — ±14V max. referred to signal common (no damage)

Normal mode rejection — at 50Hz (SDAS-8E) 40 dB min., at 60Hz (SDAS-8A) 40 dB min.

Input Offset Voltage — ±200 microvolts max.

Input Bias current — ±80nA max.
(The user's external circuit must bias the input to remain within the CMV range. The input is not isolated.)

Input Impedance — 800 kilohms, min. either input to signal common.

Resolution — 1 millivolt per count (GAIN = 1)

Analog to Digital Conversion — 12 binary bits and polarity (1 part in 8192) dual-slope conversion with auto-zeroing in the A/D converter.

PERFORMANCE

A/D Sampling Rate — Continuous transfer of all 8 channels to local memory at 15 samples/second (60 hz NMR version, SDAS-8A) or 12.5 samples/second (50Hz NMR version, SDAS-8E), jumper selected.

Highest Bandwidth — Approximately 1Hz (9600 baud, suppress clock and ident. header strings, select only one channel, polled mode). More rapid polling will re-transmit previously sent A/D samples.

Input Offset Voltage Temperature Coefficient — ±3.6 microvolts/°C max., referred to input.

Gain Temperature Coefficient — (GAIN = 1) ±20 ppm of FSR/°C typ., ±50 ppm of FSR/°C max. [voltage mode only, no TC linearization]
(external R GAIN resistor TC will add to these figures)

Accuracy (repeatability and non-linearity relative to calibration source) — ±0.02% of full scale range, ±1 count @ +25°C

Temperature Mode Accuracy (not including CJC and thermocouple calibration accuracy).

J Type	±2°C
K Type	±2°C
T Type	±2°C
S Type	±4°C

Rollover Error (Input polarity inversion, not including accuracy) ±1 Count

Calibration Control — 2 multiturn, external access potentiometers (zero and full scale gain) at edge of module, opposite connector. Recalibration is suggested every 90 days in non-hostile environments.

Internal Time of Day Clock — 23:59:59 hours:minutes:seconds (1 second resolution), ±0.05% max., ±0.01% typ. accuracy, crystal-controlled.

Cold Junction Compensation input range ..... ±99°C

COMMUNICATIONS

Data Encoding — Full Serial ASCII characters per ANSI × 3.4-1977 coding.

Baud Rates — 75, 150, 300, 600, 1200, 2400, 4800, 9600 (pin selected, see Baud rate table). Baud coding is acquired at power-up. Turn off power to reset if baud rate is changed.

Signal Levels

1. EIA RS-232-C (−3 to −15V = "1" MARK, +3 to +15V = "0" SPACE), non-isolated.
2. 20mA loop (20mA = "1" MARK, 0mA = "0" SPACE) isolated, ±2500V pk, 100 megohms*

*Current loop external excitation is required. Receiver drop: 1.6V in series with 75 ohms. Transmitter "1" drop, approx. 1.2V.

Mode — Full Duplex asynchronous, 4 wire.

Character Format — 1 Start bit (= "1"), 8 Data Bits (LSB first), no parity, 1 stop bit (= "0"), non-return to zero, compatible with terminals.

Handshake host buffer control protocol — Software only, received by SDAS-8:

XOFF = DC3 = 13 HEX = Control S
Stop SDAS-8 transmission immediate

XON = DC1 = 11HEX = Control Q
Resume SDAS-8 transmission

Hardware DSR or RTS Input to SDAS-8 is not implemented.

Distance (assuming low electrical noise environments, twisted pair or coaxial cabling):

RS-232-C	50 feet (15m)
20mA isoloop	10,000 feet (3050m)

Multidrop — Up to 4 polled stations (32D channels) may be connected in serial using two separate transmit and receive 20mA loops with external excitation (Not implemented for RS-232-C). Station selection is by station number (1 thru 4) command prefix. Auto-start or trigger start modes are not allowed.

CONTROL FEATURES

(Refer to command menu table. All commands are upper case ASCII characters plus controls)

Command Types (Input through receiver port)

1. Display formatting (line length 20, 40, 48, 72, 80, 132 char.)
2. Editing
3. A/D Channel Selection
4. A/D Data type (hex/dec radix, temperature)
5. Time-of-Day clock controls
6. Data link controls
7. Identification Header (20 characters max.)
8. Scan transmit start controls
9. Resets

Error checksum — All data strings are tagged with the hexadecimal 2's complement binary sum of the preceding data and control character string. Adding the hex values of all characters + checksum in a data string should equal zero. (This includes delimiters, syntax and controls).

Specifications, Continued

Scan Start Methods

1. Local 10 microsecond TTL trigger input
2. Polled by ASCII command
3. Auto-start using internal timer, 1 second to 17:59:59 hours interval, command selected.

POWER REQUIREMENTS

+5Vdc regulated ±5% @ 500mA max., 400mA typ.
±15Vdc regulated ±5% @ 50mA max., 30mA typ.

INPUT/OUTPUT CONNECTIONS

Pins 1, 2, 41-44 — Common logic, data and analog grounds

Pins 3, 4 + 5Vdc reg. power in.

Pin 5 +15Vdc reg. power in.

Pin 6 −15Vdc reg. power in.

Pins 7-22 — 8 Differential Analog inputs

Pin 23 — Single-ended cold junction compensation input. V_{CJC} IN = (Connector temp −0°C) × 40.96mV (see typical circuit) or use CJC module. Leave pin 23 open for non-thermocouple inputs.

Tie pin 23 to ground for external CJC.

Pin 24 — Reference out, +2.048Vdc. May be used in external ratiometric circuits to develop a common, TC-tracking system reference. An external high impedance follower would be required.

Pin 25 — A/D converter input after PGIA and multiplexer (see block diagram)

Pins 26, 27 — External resistor (mount close to connector) to increase gain up to X200. R GAIN = 20Kiloms ÷ (GAIN-1). Use a low drift precision resistor and add resistor TC to overall drift. Leave pins 26, 27 open for GAIN = 1 (FSR = ±4.095V).

Pins 28, 29, 30, 34 — Baud rate select, see chart

Pin 31 — Received Data In, RS-232-C input. Input to type 1489 circuit.

Pin 32 — Loop /$\overline{\text{RS-232-C}}$ Select input, compatible to TTL or RS-232-C levels, 2.7 kilohm pullup to +5V, type 1489 circuit.

PIN 32	20mA loop input	RS-232-C
OPEN	ENABLED	DISABLED, LEAVE OPEN
GROUND	DISABLED, INPUT = DON'T CARE	ENABLED

Pin 33 — Scan Trigger In. A local 10 microsecond positive pulse will initiate a scan transmission per the pre-selected format. Input is a 1489 circuit, compatible to TTL or RS-232-C levels. Trigger pulses sent during scan transmission will be ignored and will not be saved. Do not send trigger pulses during command inputs.

PIN 35 — Transmitted Data Out, RS-232-C output. Output from type 1488 circuit.

Pin 36-39 — 20mA serial data loop I/O. Optoisolation: 2500V pk, 100 megohms. Both ports require external excitation currents. Receiver drop 1.6V in series with 75 ohms. Transmitter "1" drop, approx. 1.2V.

Pin 40 — Request to Send Out. When the SDAS-8 emulates a modem, RTS is asserted whenever power is on. RTS should also be jumpered on the DSR and CTS lines to enable most terminals. (see block diagram).

MECHANICAL, PHYSICAL, ENVIRONMENTAL

Case Fabrication — Fully enclosed (6 sided) 2-piece steel housing.

Outline dimensions — 4" × 6" × 0.4" (101,6 × 152,4 × 10,2mm)

Mounting Method — Via 4 corner standoff holes, 4-40 threads on user's printed circuit board or 4 standoffs.

Connector — Dual in-line right angle connector, two rows of 22 square .025" pins, 0.100" spacing (row and pin — pin). Mating connector type: AMP 1-86063-8 or ITT/Cannon UBS 4-044-1D (Datel Model 60-12284-1). SDAS-8 may be adapted to flat cable headers, 3M model 609 - 4400M or equal.

Operating Temperature Range — 0 to +60°C

Storage Temperature Range — −25°C to +85°C

Weight — 10 ounces (284 grams)

ORDERING GUIDE

MODEL NUMBERING:

SDAS-8 ——

AC NORMAL MODE REJECTION AND A/D SAMPLING RATE	STATION NUMBER
A = 60 Hz (15 samples/second) E = 50 Hz (12.5 samples/second)	1 = CHANNELS 1-8 (MASTER, ECHOS ALL COMMANDS) 2 = SLAVE, CHANNELS 9-16 3 = SLAVE, CHANNELS 17-24 4 = SLAVE, CHANNELS 25-32 [USE STATIONS 2, 3, 4 ONLY IN 20mA MULTIDROP WITH STATION 1 MASTER]

Example:
SDAS-8A1

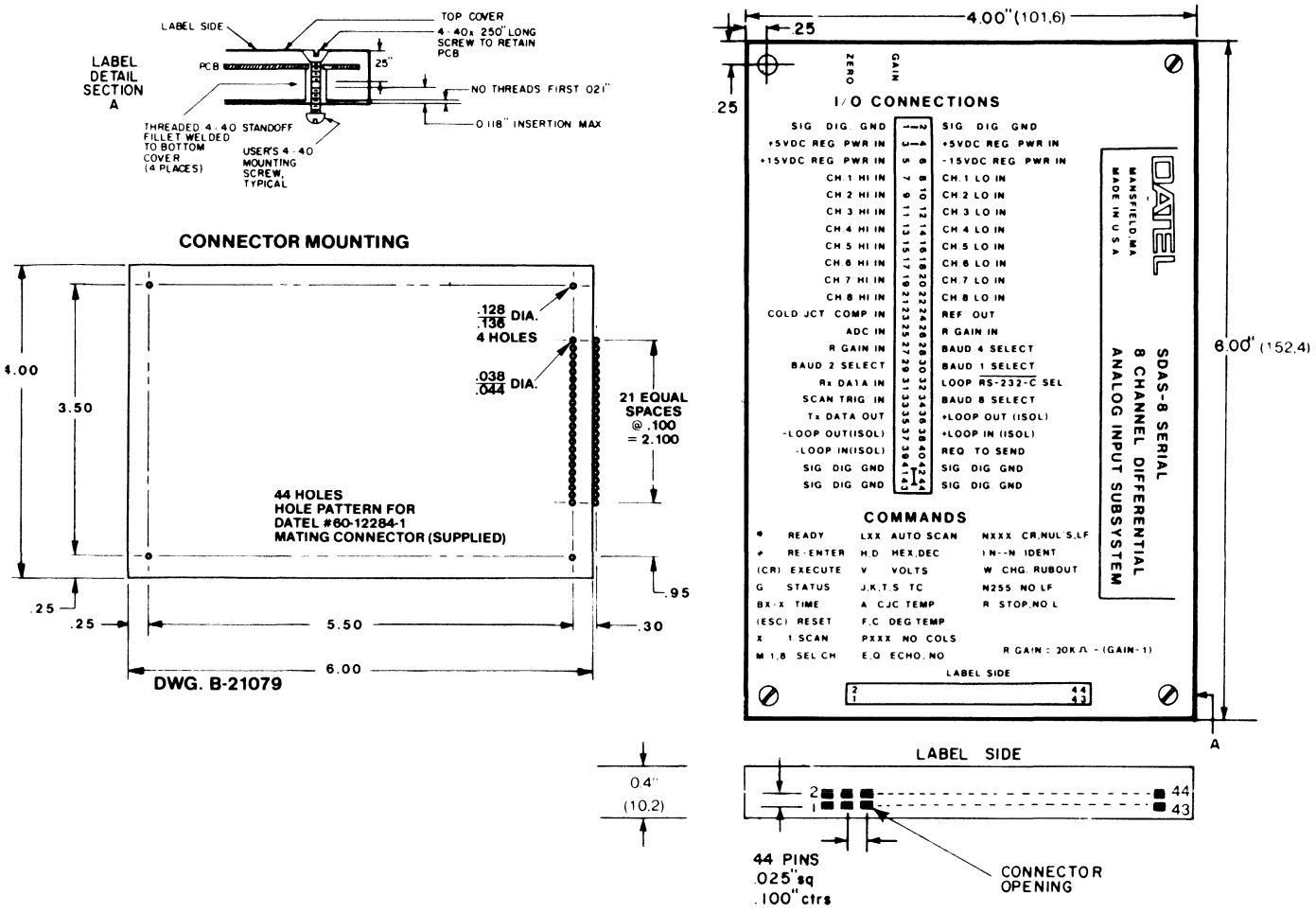
[60 Hz NMR, Master station 1, channels 1-8]

A right-angle, PCB mating connector is included.
Contact Datel for quantity discounts.

ACCESSORIES/RELATED PRODUCTS

MODEL	DESCRIPTION
60-12284-1	Spare mating connector (one is included with SDAS-8)
TPM-15/150-5/1000 (115 VAC input) TPM-15/150-5/1000E (230 VAC input) TPM-15/150-5/1000J (100 VAC input)	Modular AC power supply, 5 Vdc regulator @ 1A and ± 15 Vdc reg. @ 150 mA
58-2079260	DB-25P solder tab RS-232-C connector
ST-705A (115 VAC/60 Hz) ST-705E (230 VAC/50 Hz) ST-705J (100 VAC/50 Hz)	Complete SDAS-8 subsystem, AC power supply, screw terminal inputs, CJC amplisensor, DB-25 connector
MPP-20, 48 Printers	Request Brochures

Mechanical Dimensions — Inches (mm)



A/D CODING TABLE

Input Volts (R GAIN = ∞) (no connection)	Hexadecimal Display*	Decimal Display
+4.096 V	+++++	+++++
+4.095 V	ØFFFH	+4.095
+2.048 V	Ø800H	+2.048
+1.024 V	Ø400H	+1.024
+0.256 V	Ø100H	+0.256
+0.002	Ø010H	+0.002
+0.001	Ø001H	+0.001
0.000	0000H	+0.000
−0.001	FFFFH	−0.001
−0.002	FFFEH	−0.002
−0.256 V	FF00H	−0.256
−1.024 V	FC00H	−1.024
−2.048 V	F800H	−2.048
−4.095 V	F001H	−4.095
−4.096 V	-----	-----

*In hex, the polarity bit 12 has been extended to the top 3 MSB's (Bits 13, 14, 15)

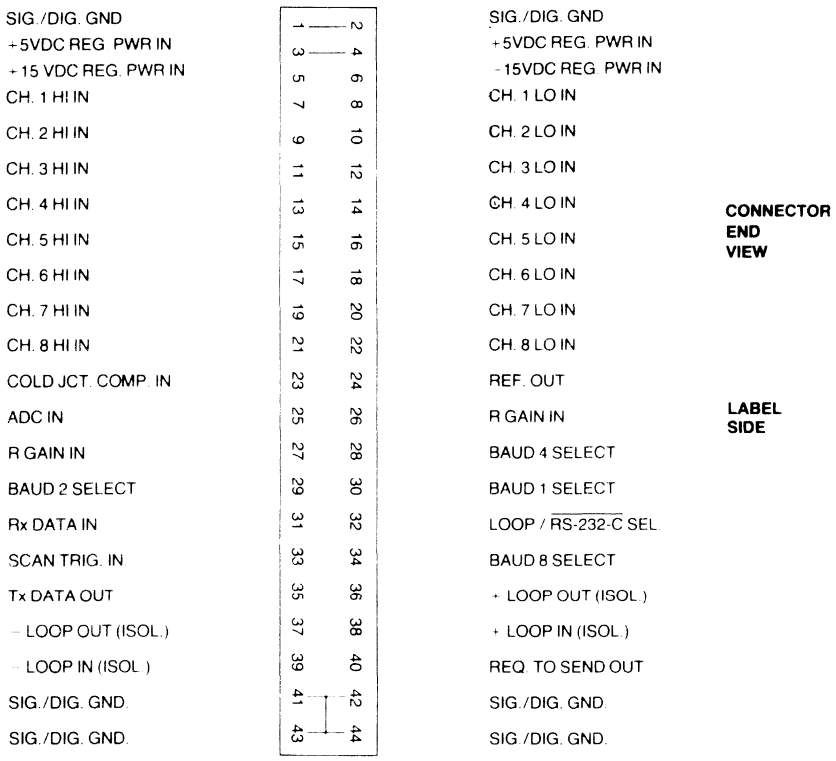
BAUD RATE SELECTION TABLE

Where Baud Rate = 1 ÷ Bit Period (in seconds) and logic "1" = +5V or open; "0" = ground or zero volts

BAUD RATE	BAUD SEL. 8 (pin 34)	BAUD SEL. 4 (pin 28)	BAUD SEL. 2 (pin 29)	BAUD SEL. 1 (pin 30)
75	1	0	0	1
150	1	0	0	0
300	0	1	1	1
600	0	1	1	0
1200	0	1	0	1
2400	0	1	0	0
4800	0	0	1	1
9600	0	0	1	0

INPUT/OUTPUT CONNECTIONS

R GAIN = 20KΩ ÷ (GAIN-1)



DATA LINK HANDSHAKING

SDAS-8 uses a minimal subset of the EIA RS-232-C I/O line designation (refer to the block diagram), consisting of Transmitted Data, Received Data, Signal Ground and Protective Ground. SDAS-8 also supplies an RS-232-C level Request-to-Send output which is always asserted when power is applied. Users may also need to assert the Data Set Ready input to the terminal or computer.

Otherwise, it is assumed that SDAS-8 will be used full duplex and all handshaking is data-encoded. Users who must operate half-duplex may suppress normal character echo from SDAS-8 back to the display by using the Q (CR) command. Users would normally write their computer program to change a half-duplex line from transmit to receive after the X (CR) scan command is sent with the echo suppressed. After a polled (X command) A/D scan was received, the host should turn the line around to transmit to be ready for the next command.

SDAS-8 also interprets the XOFF/XON protocol (control S or DC3/control Q or DC1) to intermittently halt the SDAS-8 transmitter in mid-string. This is used with computers which have a limited input string buffer length to prevent buffer overflow.

Send Escape first when operating SDAS-8 from a terminal

User's who wish to operate SDAS-8 manually from a CRT or printer terminal or from a microcomputer which is emulating an ASCII terminal should first send an Escape character to remove SDAS-8 from the power-up printer mode. This mode is intended for direct connection to Datel's APP-20 and APP-48 miniature thermal printers using the triggered scan start. These printers require suppression of Line Feed and 216 NUL characters following the Carriage Return to allow time to print each line. Sending an Escape after power-up reinstates the Line Feed following Carriage Return and cancels the filler NUL's.

ERROR DETECTION

All data is tagged with a 4-character hexadecimal checksum. The 16-bit (4 ASCII hex character) checksum is a 2's complement sum of all the previous data and control characters sent in the string before the checksum characters (the MSB bit 7 in each previous character is set to zero). By adding the checksum to the string sum, a zero result will indicate no data errors. Normally a user's program should perform this addition and CALL an error-flagging subroutine if the algebraic result is not zero. If the data link reliability is high, or occasional data errors are tolerable, this procedure is not required.

DISPLAY FORMATTING

For highest data efficiency, data is packed with a minimum of formatting characters. Normally, for data logging or display applications, the user would format the data (arrange it in tabular columns), apply labels ("gallons per hour," "RPM," "pump No. 4" etc.) and apply offset and span scaling arithmetic to the data. This is best done in the user's computer, probably using high-level language such as BASIC or FORTRAN which have display/printout formatting syntax.

Using SDAS-8 with Datel's MPP-20 and APP-48A2 Printers

When SDAS-8 is first powered up, either of these full serial RS-232-C printers may be directly connected and operated in the triggered scan mode with a TTL start pulse to SDAS-8 pin 33. The 216 NUL filler characters following CR allow adequate time for the 750mS print cycle *provided that 2400 BAUD or lower is selected.* In addition, the printer connector jumpering and DIP switches must also match the SDAS-8 word format (8 data, no parity, 1 stop).

SERIAL COMMAND SUMMARY

LEGEND:

1. XXX — X are characters entered and displayed on the terminal.
2. ( ) are blind control characters (such as carriage return or escape) which do not appear on the terminal.
3. [ ] are notes on the command. They are not entered or displayed.
4. Carriage return (CR) requests the SDAS-8 to execute the command consisting of the previous character string.
5. The asterisk (*) confirms that the command was executed, and is ready for the next command.
6. The pound sign (#) indicates that the returned character string is not executable. Re-enter a corrected string.

COMMAND CHARACTERS

G (CR) — Display status message
B (CR) — Display time (HR: MIN: SEC)
B 23:59:59 (CR) — Set time in 24 hour format
(Escape) — Reset all controls to power-up status except clock
(Backspace) — Delete previous character
(Control S or DC3 or XOFF) — [13 HEX] Stop transmission immediate and wait
(Control Q or DC1 or XON) — [11 HEX] Start transmission immediate, mid-string
R — Stop output transmission from SDAS-8.
Stop L mode auto-start timer. (CR) not required. Revert to trigger or polled-start mode.

A/D CONTROLS

X (CR) — Display one scan
M:2 (CR) — Set up to display channel 2 only
M:1, 8 (CR) — Set up to display channels 1-8
LO2 (CR) — Start automatic scan transmissions every 2 seconds. R or (ESC) are the only way to stop L mod.
L59:59 (CR) — Start automatic scan transmissions every 59 minutes :59 seconds
L17:59:59 (CR) — Start automatic scan transmissions every 17:59:59 hours: minutes / seconds (max).
H (CR) — Format A/D data as hexadecimal ASCII
D (CR) — Format A/D data as decimal ASCII (cancel hex)
V (CR) — Format A/D data as DC volts, (cancel thermocouple)
J (CR) —Format A/D data linearized to selected thermocouple
K (CR)
S (CR)
T (CR)

* — Power-up prompt. Previous command executed; ready for next command.
# — Echoed string not executable; try again.

A (CR) — Transmit A/D data from CJC channel, equivalent ambient temperature. Range ±99°C
F (CR) — Format A/D data as Fahrenheit.
C (CR) — Format A/D data as Celsius.

TERMINAL CONTROLS

W (CR) — Toggles between rubout echo as BS-SP-BS or /X where X is the last character.
P80 (CR) — Set column width to 20, 40, 48, 72, 80 or 132 (20 = power up state)
E (CR) — Echo all printables (power up state) for full duplex
Q (CR) — Don't echo printables (for half duplex)
N nnn (CR) — Insert nnn nulls between, CR, NULL's, LF
N255 (CR) — Suppress line feed. End all scans with CR, (NULL's), no line feed, N255 (CR) is a toggle, which cycles on and off with each application. Confirm the line feed status bit using the G status.

IDENT STRING

I : nnn — n (CR) — Start all A/D scans with the Ident character string nnn — n (20 characters max)
All lower case printables — Echo if selected. Not acted upon.
All non-specified controls — Echo if selected. Not acted upon.
BN (CR) — Delete, time and station
BY (CR) — Resume, time and station

POWER UP MODE

Station 1
20 characters per line
Trigger/polled scan start
8 channels, 1-8
Echo on

Elapsed time from power-on
The line terminator sequence at power up is:
<CR, NUL, NUL, -- (216 NUL's), no LF>
For CRT's, send ESCAPE to cancel the NUL's and restore LF.

DATA OUTPUT FORMAT

The following message samples were prepared on an SDAS-8 directly connected to an RS-232-C Datel APP-48A2 thermal printer and a CRT terminal. These data printouts indicate the degree of formatting control, channel selection, editing and message readability offered by SDAS-8. Note throughout these samples the visual format consistency even when changing line length. Each data point uses a constant 9 characters and is tagged with a hex checksum for optional error detection. Hexadecimal samples always include an "H" in the data with optional C or F temperature tags trailing the H. The suppressable clock line includes the station number and an optional 20-character ident/header message is returned with each sample (4 headers may be used with 4 multidrop stations).

While some computer programs may re-format returned data strings, many will simply reflect the string out to a printer or other ASCII device. SDAS-8 data will preserve the consistent readability of this output.

ASCII Controls which are blind (CR, LF, NUL's, DEL, ESCAPE, etc.) of course are not displayed but their effects can be seen in the editing and non-executable command strings.

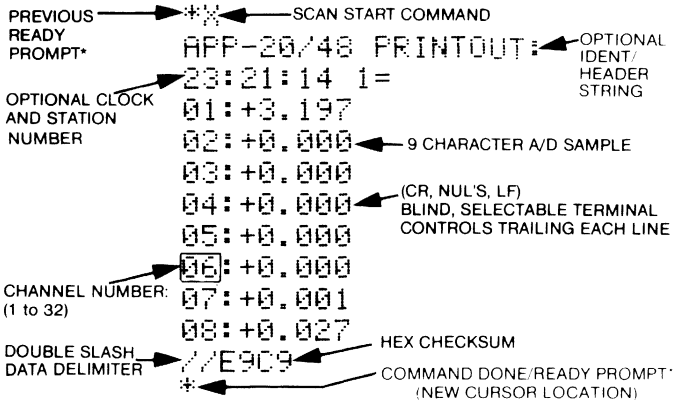
LOADING AN IDENT/HEADER STRING:

```
*I:APP-20/48 PRINTOUT:
```

SETTING AND DISPLAYING THE CLOCK:

```
*B23:00:00
*B
23:00:02
```

20-COLUMN OUTPUT:



40-COLUMN OUTPUT USING THE IDENT/HEADER AS A DATE STAMP WITH FAHRENHEIT THERMOCOUPLE PRESENTATION:

```
*%
10/17/83 BATCH 9
23:15:56 1=
01:+1824F/02:  +83F/03:  +83F
04:  +83F/05:  +83F/06:  +83F
07:  +83F/08:  +97F//EAB9
```

STATUS MESSAGE:

```
*G
B80481/ HEX STATUS
STATION 1 ONLINE
TIME 23:07:15
40 CHARS PER LINE
START CHAN. IS 1
FINAL CHAN. IS 8
TYPE J THERMOCOUPLE
ECHO IS ON
OUTPUT IS HEX. DEG F
DEL ECHOED /LAST CHR
NO LF AFTER CR
```

AMBIENT CJC CELSIUS DECIMAL OUTPUT:

```
*A
SDAS-8 IDENT STRING
23:10:13 1=
CJC:  +27C//F9B3
```

RESPONSE TO NON-EXECUTABLE COMMAND STRING:

```
*BAD COMMAND SAMPLE
BAD COMMAND SAMPLE#
```

RESPONSE TO PRINTER-COMPATIBLE BACKSPACE FUNCTION:

```
*DEL/L/E/D
```

48-COLUMN CELSIUS THERMOCOUPLE OUTPUT:

Note: Terminate each line entered from the keyboard with carriage return.

```
*%
IBM PC SDASLOGGER
23:22:00 1=
01: +736C/02:  +29C/03:  +29C/04:  +29C
05:  +29C/06:  +29C/07:  +29C/08:  +35C
//E949
```

HEXADECIMAL CELSIUS OUTPUT AFTER SELECTING CHANNELS 1-3:

```
*M:1,3
*%
LO PRESS TURBO TEMP
00:30:12 1=
01:02E0HC/02:001CHC/03:001CHC//F1DF
```

HEX VOLTS OUTPUT, CHANNELS 1-3:

```
*%
MANIFOLD GAL/HR
00:30:20 1=
01: 0C7EH/02: 0000H/03: 0000H//F259
```

STATUS MESSAGE FORMAT

In response to a G (CR) command (or 2G, 3G, 4G for Multidrop stations), SDAS-8 will transmit a status message in 20 column format. The status message contains two parts: an encoded hexa-decimal header and a plain-English body. The header may be read by the user's host computer (after being intercepted by a string-capture parsing program) and the body is eyeball-compatible.

The status message indicates the contents of 3 status bytes (24 bits) which SDAS-8 assembles when status is requested. The 3 bytes are represented by 6 ASCII hex characters such that the least significant 4-bit hex nybble of each ASCII hex character comprise the upper and lower nybbles of each of the 3 bytes.

Two of the status bytes indicate various formatting parameters and the third byte indicates A/D channel selection for that station.

The encoded hex status is placed at the beginning of the message to simplify the task of the user's parsing program (to avoid searching the entire message string for status information).

At power-up, the status defaults to the state shown including 216 filler NUL's after CR and suppression of line feed. An Escape command sent anytime thereafter reverts to this default state *except* that the NUL's are deleted and LF is inserted after CR.

Status Message format (□ = variable)

[FFFFF]/HEX STATUS <CR, NULS, LF>
STATION [1] ON LINE <CR, NULS, LF>
[20] CHARS. PER LINE <CR, NULS, LF>
[TRIGGER / TIMER] SCAN START <CR, NULS, LF>
START CHAN. = [1] <CR, NULS, LF>
FINAL CHAN. = [8] <CR, NULS, LF>
TYPE [J] THERMOCOUPLE <CR, NULS, LF>: not listed on default
ECHO IS [ON / OFF] <CR, NULS, LF>
OUTPUT = [DEC. / HEX.] VOLTS / DEG. C <CR, NULS, LF>
BS = [/ LAST CHAR. / BS-SP-BS] <CR, NULS, LF>
[LF ADDED AFTER CR <CR, NULS, LF> / NO LF AFTER CR]

Encoded HEX Status:

FFFFFF/HEX STATUS <CR, NULS, LF>
- CHAN. SELECT BYTE (HI CHAN., LO CHAN.)
- 2ND STATUS BYTE
- 1ST STATUS BYTE

Power up default state will be: 000081

1st Status Byte

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	— DEFAULT STATE

BITS 1 + 0 — 00 For J type thermocouples (default state)
— 01 For K type thermocouples
— 10 For S type thermocouples
— 11 For T type thermocouples
BIT 2 — 0 = ECHO ON (default state)
— 1 = ECHO OFF
BIT 3 — 0 = Output in volts [default] [overrides bits 0+1+5]
— 1 = Output in temperature
BIT 4 — 0 = Output in Decimal (default state)
— 1 = Output in Hexadecimal
BIT 5 — 0 = Output in Celcius (default)
— 1 = Output in Fahrenheit
BIT 6 — 0 = Rubout or Backspace as / last char.(default)
— 1 = Rubout as BS-SP-BS sequence
BIT 7 — 0 = LF enabled after fill characters
— 1 = LF disabled after CR (default)

2nd Status Byte

7	6	5	4	3	2	1	0	
0	X	0	0	0	0	0	0	— DEFAULT STATE

BITS 1+0 — 00 = Communicating with station 1 (default)
— 01 = Communicating with station 2
— 10 = Communicating with station 3
— 11 = Communicating with station 4
BITS 4+3+2 — 000 = 20 Characters per line (default)
— 001 = 40 Characters per line
— 010 = 48 Characters per line
— 011 = 72 Characters per line
— 100 = 80 Characters per line
— 101 = 132 Characters per line
BIT 5 — 0 = Trigger or polled start mode (default)
— 1 = Timer start mode
BIT 6 — Don't care
BIT 7 — 0 = XON SET (default)
— 1 = XOFF SET

3rd Channel Selection Byte

7	6	5	4	3	2	1	0	
1	0	0	0	0	0	0	1	— DEFAULT STATE

BITS 0+1+2+3 — Low channel scan selection
BITS 4+5+6+7 — High channel scan selection

MULTIDROP APPLICATIONS

This application shows up to four multidrop SDAS-8 stations sharing common transmit and receive 20mA serial data loops. Because each T/R serial port is optically isolated, the internal analog channels may have several hundred volts of isolation from station to station (*within* a single station however, analog inputs must remain within the ±11V common mode voltage range). By using the current loop mode, stations may be separated thousands of feet in low noise environments. The two current loops require a source of excitation and a typical circuit and external power supply is shown. Some host computers and terminals include their own excitation supplies. Users should carefully test such remote systems because low data errors are a complex result of shielding, noise protection, wire type, baud rate, and link ringing suppression.

Multidrop SDAS-8 stations are addressed with a station number prefix before each command (Example: "3M:2(CR)" configures station 3 (channels 17-24) to respond with only channel 18 in returned data strings). Ommission of the station number prefix always implies station 1 (channels 1-8), which responds with or without the 1 prefix.

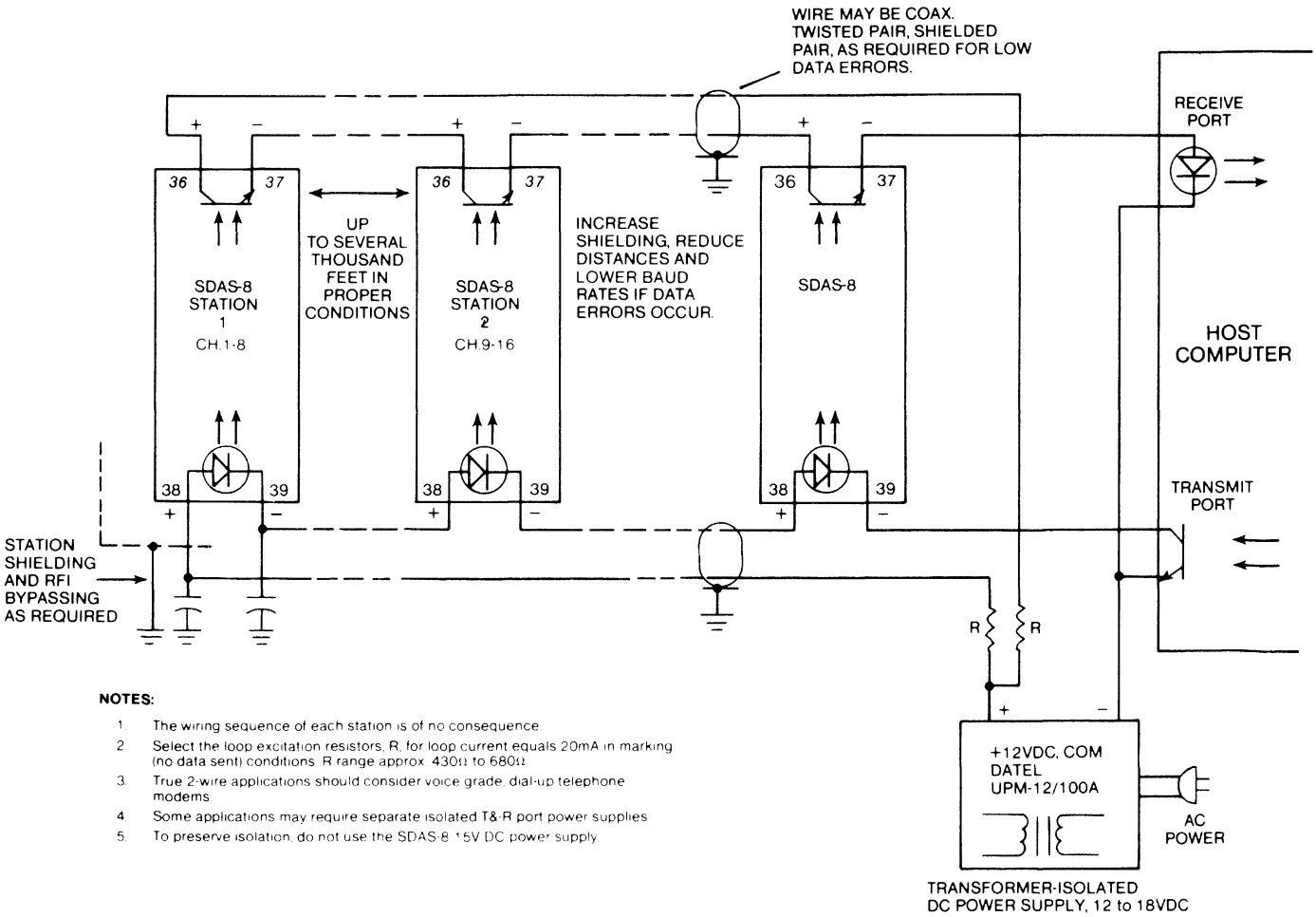
In multidrop applications, separate stations may have differing identification header strings and the station number is always included at the end of the clock line.

Self start auto scans (L mode) are not allowed in multidrop applications, to avoid data collisions on the host computer's receive port. Locally triggered scan starts are also not advisable in multidrop. Normal multidrop applications should use a polled mode, "4X(CR)" for each station.

Multidrop allows a mix of different gains and transducer types from station to station. Longer distance applications or those demanding only two wires or applications where installing more wires is unsuitable should consider using auto-answer RS-232-C modems and either telephone or radio links.

The serial loop port circuits shown for each SDAS-8 station have been simplified for this drawing. The actual circuits contain some additional protection not shown for miswiring abuse (reverse polarity clamps, current limiters, etc.).

TYPICAL 20mA ISOLATED SERIAL LOOP MULTIDROP WIRING, 4 CONDUCTOR



NOTES:

1. The wiring sequence of each station is of no consequence.
2. Select the loop excitation resistors, R, for loop current equals 20mA in marking (no data sent) conditions. R range approx. 430Ω to 680Ω.
3. True 2-wire applications should consider voice grade, dial-up telephone modems.
4. Some applications may require separate isolated T&R port power supplies.
5. To preserve isolation, do not use the SDAS-8 +5V DC power supply.

Selected New Products

3.5 DIGIT, MINIATURE VOLTAGE METERS

	Model	Power	Std. Input	Case	Features
NEW **Self-Contained 3.5 Digit LED Ultra-Miniature**	**DMH-30PC-0**	+5Vdc	±200 mV	A	Encapsulated (Plastic), 24-pin DDIP
	DMH-30PC-1	+5Vdc	±2Vdc	A	Encapsulated (Plastic), 24-pin DDIP
	DMH-30PC-2	+5Vdc	±20Vdc	A	Encapsulated (Plastic), 24-pin DDIP
	DMH-30MM-0	+5Vdc	±200mV	A	Hermetically Sealed, Quartz window, Ceramic 24-pin DDIP, MIL-D-87157 Temperature Range
	DMH-30MM-1	+5Vdc	±2Vdc	A	
	DMH-30MM-2	+5Vdc	±20Vdc	A	
NEW **Self-Contained Single-Piece 3.5 Digit LED**	**DMS-30PC-0-RL**	+5Vdc	±200mV	B	Sealed, Plastic Case, Low Power RED Display
	DMS-30PC-1RL	+5Vdc	±2Vdc	B	
	DMS-30PC-2-RL	+5Vdc	±20Vdc	B	
	DMS-30PC-0-RS	+5Vdc	±200mV	B	Sealed, Plastic Case, Standard Intensity RED Display
	DMS-30PC-1-RS	+5Vdc	±2Vdc	B	
	DMS-30PC-2-RS	+5Vdc	±20Vdc	B	
	DMS-30PC-0-RH	+5Vdc	±200mV	B	Sealed, Plastic Case, High Intensity RED Display
	DMS-30PC-1-RH	+5Vdc	±2Vdc	B	
	DMS-30PC-2-RH	+5Vdc	±20Vdc	B	
	DMS-30PC-0-GL	+5Vdc	±200mV	B	Sealed, Plastic Case, Low Power GREEN Display
	DMS-30PC-1-GL	+5Vdc	±2Vdc	B	
	DMS-30PC-2-GL	+5Vdc	±20Vdc	B	
	DMS-30PC-0-GS	+5Vdc	±200mV	B	Sealed, Plastic Case, Standard Intensity GREEN Display
	DMS-30PC-1-GS	+5Vdc	±2Vdc	B	
	DMS-30PC-2-GS	+5Vdc	±20Vdc	B	
	DMS-30PC-0-AS	+5Vdc	±200mV	B	Sealed, Plastic Case, Standard Intensity AMBER Display
	DMS-30PC-1-AS	+5Vdc	±2Vdc	B	
	DMS-30PC-2-AS	+5Vdc	±20Vdc	B	
	DMS-30PC-0-YS	+5Vdc	±200mV	B	Sealed, Plastic Case, Standard Intensity YELLOW Display
	DMS-30PC-1-YS	+5Vdc	±2Vdc	B	
	DMS-30PC-2-YS	+5Vdc	±20Vdc	B	
	DMS-30PC-0-OH	+5Vdc	±200mV	B	Sealed, Plastic Case, High Intensity ORANGE Display
	DMS-30PC-1-OH	+5Vdc	±2Vdc	B	
	DMS-30PC-2-OH	+5Vdc	±20Vdc	B	
NEW **Self-Contained Single-Piece 3.5 Digit LCD**	**DMS-30LCD-0/5**	+5Vdc	±200mV	C	Sealed, Plastic Case
	DMS-30LCD-1/5	+5Vdc	±2Vdc	C	
	DMS-30LCD-2/5	+5Vdc	±20Vdc	C	
	DMS-30LCD-0/9	+9 to +15Vdc	±200mV	C	Sealed, Plastic Case, Suitable for battery operation
	DMS-30LCD-1/9	+9 to +15Vdc	±2Vdc	C	
	DMS-30LCD-2/9	+9 to +15Vdc	±20Vdc	C	

CASE SIZES
A 1.29"W x 0.25"D x 0.80"H (33 x 6 x 20 mm)
B 2.19"W x 0.54"D x 0.95"H (55 x 14 x 24 mm)
C 2.16"W x 0.66"D x 0.92"H (55 x 16 x 24 mm)

3 1/2 DIGIT DIGITAL PANEL METERS

	Model	Power	Std. Input	Case*	Features
3.5 Digit LED	DM-3100L-1	+5Vdc	±2Vdc	B	Short Depth Case
	DM3100N-1	+5Vdc	±2Vdc	A	Provisions for 4-20 mA input
	DM-3101-1	+5Vdc	±2Vdc	A	High Intensity Display
	DM3103-1	+5Vdc	±2Vdc	B	High Intensity Display
	DM-31-1	+5Vdc	±2Vdc		Low Cost - Uncased
	DM-3100B-1	115/230VAC	±2Vdc	B	Short Depth Case
	DM3104-1	115/230VAC	±2Vdc	B	High Intensity Display
	DM-9115-1	115/230VAC	±2Vdc	C	NEMA 12 (Vibration Std)
3.5 Digit LCD	DM-3100U-1	+5/9Vdc	±2Vdc	A	Units Display (Batt. Pwr.)
	DM-3100X-1	+5/9Vdc	±2Vdc	B	Battery Powered
	DM-3102A	+5Vdc	±2Vdc	A	Units Display Autoranging (200 mV - 200V)
	DM-LX3-1	+5Vdc	±2Vdc		Low Cost - Uncased
	DM-3100U2	115VAC	±2Vdc	A	Units Display
Other Digital Panel Products	DBM-20	+5Vdc	Adjustable	A	20 Segment LED Bar Graph w/ TTL Outputs
	PC-6	+5Vdc		B	10 MHz Counter/Timer

NOTE: Input range kits are available for all DM-3100, 4100, and 9000 Series DPMs

* Refer to page 67 for actual dimensions

4 1/2 DIGIT DIGITAL PANEL METERS

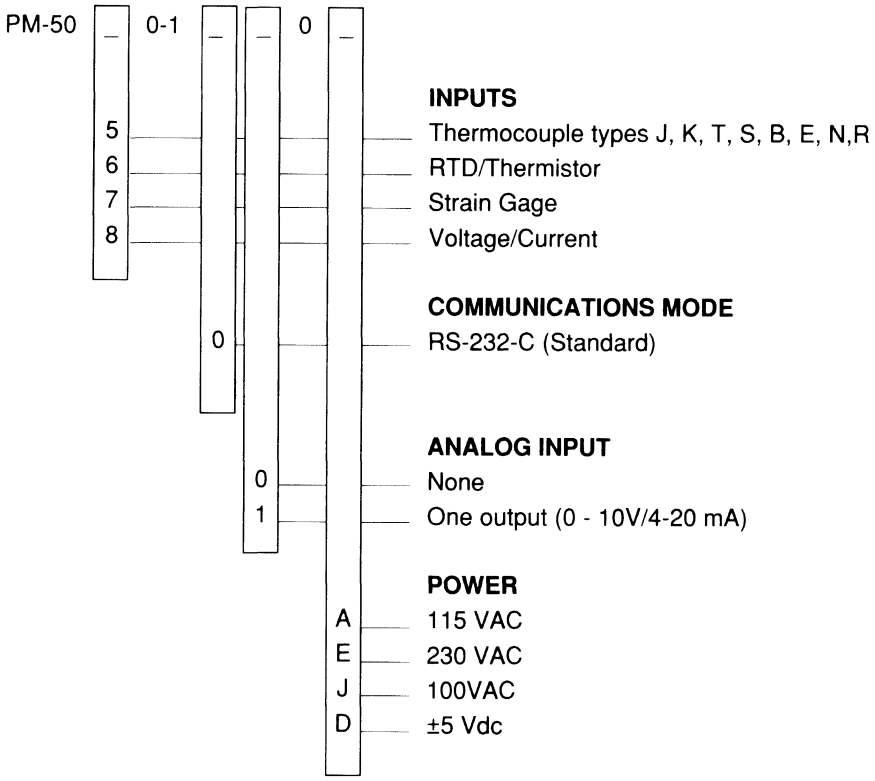
	Model	Power	Std. Input	Case*	Features
4.5 Digit LED	DM-4101N-1	+5Vdc	±2Vdc	A	High Intensity Display
	DM-9200-1	+5Vdc	±2Vdc	C	NEMA 12 (Vibration Standard)
	DM-4100D-1	+5Vdc	±2Vdc	A	High Speed Sampling Serial/ParallelBCD Output
	DM-4101D-1	+5Vdc	±2Vdc	A	High Intensity Display Serial/Parallel BCD Output
	DM-4101L-1	+5Vdc	±2Vdc	B	Serial BCD Output
	DM-4200-1	+5Vdc	±2Vdc	A	Serial BCD Output
	DM-9215-1	115/230VAC	±2Vdc	C	NEMA 12 (Vibration)
4.5 Digit LCD	DM-4105-1	+5Vdc	±2Vdc	A	Serial BCD OUT (Batt. Pwr.)
Other Digital Panel Products	DBM-20	+5Vdc	Adjustable	A	20 Segment LED Bar Graph w/ TTL Outputs
	PC-6	+5Vdc		B	10 MHz Counter/Timer

NOTE: Input range kits are available for all DM-3100, 4100, and 9000 Series DPMs

* Refer to page 67 for actual dimensions

PROCESS MONITORS/CONTROLLERS

DATEL designs and manufactures a complete line of Process Monitors/Controllers supporting Thermocouples, RTDs, Strain Gages, and Voltage/Current signal inputs. These low cost units contain such features as built-in RS-232 serial port, user-selectable setpoint outputs (up to 4 discrete and 1 optional Analog), built-in configuration and setup command set, fully isolated inputs (to 1500 Volts, typ.) and a six-character, 14-segment vacuum fluorescent display (blue-green). Each model may be configured and operated from either the front panel or via the serial port. For reliability, accuracy, and low price, DATEL's PM-5000 Series Process Monitors/ Controllers are simply the best.



VOLTAGE CALIBRATORS

MODEL	OUTPUT RANGE	SETTABLE INCREMENTS	ACCURACY	SOURCE/SINK CURRENT	DISPLAY	POWER	CASE/ MOUNTING
DVC-350A	±1.2000 or ±12.000	100 μV or 1 mV	0.015%	20 mA	4 1/2 DIGIT LCD	9V Battery or 115 VAC Adaptor (optional)	5.75 X 3.60 X 1.29 in (146 X 91 X 33 mm) HAND HELD
DVC-8500	±19.999	1 mV	0.005%	25 mA	4 1/2 DIGIT MECHANICAL	100 VAC (J) 115 VAC (A) 230 VAC (E)	5.59 X 2.11 X 5.78 (142 X 54 X 147 mm)

PANEL MOUNT THERMAL PRINTERS

Model	Columns	Input Interface	Power (Note 1)	Character Set	Case*	Special Features
DPP-Q7	7	BCD	115/230 VAC	Numeric (decimal or hex) plus sign	A	Simple DATEL DPM interface
APP-20A1	20	Parallel	115/230 VAC	96 char ASCII	A	Inverted, tall character options
APP-20D1	20	Parallel	+12 Vdc	96 char ASCII	A	Inverted, tall character options
APP-20A21	20	RS-232/20 mA loop	115/230 VAC	96 char ASCII	A	Inverted, tall, condensed character options
APP-20A21	20	RS-232/20 mA loop	+12 Vdc	96 char ASCII	A	
APP-20D21	20	IEEE-488	115/230 VAC	96 char ASCII	A	Inverted, tall character options
MPP-20A	20	RS-232/Parallel	115 VAC	127 char ASCII	A	Inverted, tall, enhanced character options
MPP-20D	20	RS-232/Parallel	+12 Vdc	127 char ASCII	A	
MPP-20E	20	RS-232/Parallel	230 VAC	127 char ASCII	A	
APP-48A1	48	Parallel	115 VAC	192 char ASCII	B	Inverted character options
APP-48A2	48	RS-232	115/230 VAC	192 char ASCII	B	Inverted character options
APP-48D2	48	RS-232	+12 Vdc	192 char ASCII	B	Inverted character options
APP-48A3	48	IEEE-488	115/230 VAC	192 char ASCII	B	Inverted character options
APP-48D3	48	IEEE-488	+12 Vdc	192 char ASCII	B	Inverted character options
APP-M20A1	20	Parallel	115/230 VAC	96 char ASCII	C	Hardened for shock, vibration and humidity (mobile)
APP-M20A21	20	RS-232	115/230 VAC	96 char ASCII	C	
APP-M20D21	20	RS-232	+12 Vdc	96 char ASCII	C	
APP-M48D1	48	Parallel	+12 Vdc	192 char ASCII	D	
APP-M48D2	48	RS-232	+12 Vdc	192 char ASCII	D	
NEW **GPP-42**	42	Serial/Parallel	115/230 VAC (50/60 Hz)	256 char ASCII	E	8 International Character Sets High Res Graphics, 200 Line Buffer CUSTOM CHARACTERS AVAILABLE

NOTE 1. 100 VAC versions available for most models ("J" version); European line cords also available ("E" version). Consult factory.

CASES* Refer to pages 163 to 168 for dimensional drawings.

A = 4.44"W x 2.76"H x 8.00"D
B = 8.20"W x 2.84"H x 8.14"D
C = 5.36"W x 3.74"H x 8.00"D (Including mobile-mount brackets)
D = 9.25"W x 3.25"H x 10.44"D (Including mobile-mount brackets)
E = 8.20"W x 2.84"H x 10.50"D

Advanced Technology A/D Conversion Components Summary Tables

SAMPLING A/D CONVERTERS

	Model	Resolution (Bits)	Throughput (MHz)	Linearity Error (Max)	Power Watts (Max)	Case
	ADC-HS12B	12	0.066	±3/4 LSB	1.8	32-Pin DIP
	ADS-111	12	0.500	±3/4 LSB	1.8	24-Pin DIP
	ADS-112	12	1.0	±3/4 LSB	1.7	24-Pin DIP
	ADS-193	12	1.0	±3/4 LSB	1.7	40-Pin DIP
	ADS-21PC	12	1.3	±1 LSB	2.5	46-Pin DIP
	ADS-132	12	2.0	±3/4 LSB	3.2	32-Pin DIP
Preliminary	**ADS-117**	12	2.0	±3/4 LSB	1.8	24-Pin DIP
Preliminary	**ADS-118**	12	5.0	±1 LSB	2.5	24-Pin DIP
	ADS-131	12	5.0	±1 LSB	4.0	40-Pin DIP
	ADS-130	12	10.0	±1 LSB	4.2	40-Pin DIP
Advanced	**ADS-120**	12	20.0	±1 LSB	4.2	40-Pin DIP
	ADS-924	14	0.300	±1 LSB	1.8	24-Pin DIP
	ADS-928	14	0.500	±3/4 LSB	3.4	32-Pin DIP
Preliminary	**ADS-941**	14	1.0	±3/4 LSB	3.3	32-Pin DIP
Preliminary	**ADS-942**	14	2.0	±1 LSB	3.4	32-Pin DIP
Advanced	**ADS-944**	14	5.0	±1 LSB	3.4	40-Pin DIP
Advanced	**ADS-945**	14	10.0	±1 LSB	4.2	40-Pin DIP
Advanced	**ADS-976**	16	0.200	±2 LSB	1.8	32-Pin DIP
Preliminary	**ADS-930**	16	0.500	±1 1/2 LSB	2.4	40-Pin DIP

A/D CONVERTERS

	Model	Resolution (Bits)	Conversion Time (µsec)	Linearity Error	Power (Watts)	Case
	ADC-207	7	0.050	±1/2 LSB	0.25	18-Pin DIP
	ADC-228	8	0.040	±1/2 LSB	1.25	24-Pin DIP
	ADC-208	8	0.050	±3/4 LSB	0.60	24-Pin DIP
	ADC-304	8	0.050	±1/2 LSB	0.39	28-Pin DIP
New	**ADC-530**	12	0.350	±3/4 LSB	2.10	32-Pin DIP
	ADC-500	12	0.500	±1 LSB	1.70	32-Pin DIP
	ADC-505	12	0.550	±1 LSB	1.70	32-Pin DIP
	ADC-508	12	0.700	±1 LSB	1.70	32-Pin DIP
	ADC-520	12	0.800	±1/2 LSB	1.60	32-Pin DIP
	ADC-521	12	0.800	±1/2 LSB	1.60	32-Pin DIP
	ADC-511	12	1.0	±3/4 LSB	1.25	24-Pin DIP
	ADC-HZ12B	12	8	±1/2 LSB	1.5	32-Pin DIP
	ADC-HX12B	12	20	±1/2 LSB	1.5	32-Pin DIP
	ADC-HC12B	12	300	±1/2 LSB	0.17	32-Pin DIP
	ADC-908	14	1.0	±1/2 LSB	2.70	32-Pin DIP
	ADC-914	14	2.4	±1 LSB	1.20	24-Pin DIP

D/A CONVERTERS

Model	Resolution (Bits)	Settling Time	Linearity Error	Power (Watts)	Case
DAC-HF8	8	25 ns	±1/2 LSB	0.750	24-Pin DIP
DAC-HF10	10	25 ns	±1/2 LSB	0.900	24-Pin DIP
DAC-HF12	12	50 ns	±1/2 LSB	0.900	24-Pin DIP
DAC-HK12	12	3 µs	±1/2LSB	0.700	24-Pin DIP
DAC-HZ12	12	3 µs	±1/2 LSB	0.390	24-Pin DIP
DAC-HP16	16	15 µs	±0.003% FSR	0.600	24-Pin DIP

SAMPLE HOLD AMPLIFIERS

	Model	Linearity (%)	Acquisition Time	Aperture Delay	Aperture Jitter	Bandwidth (MHz)	Hold Mode Droop	Case
	SHM-HU	0.1	25 ns	6 ns	10 ps	50	50 µV/µs	24-Pin DIP
	SHM-7	0.1	40 ns	3 ns	10 ps	40	100 µV/µs	24-Pin DIP
	SHM 40	0.1	40 ns	3 ns	10 ps	40	100 µV/µs	24-Pin DIP
	SHM-6	0.02	2 µs	20 ns	2 ns	5	10 µV/µs	32-Pin DIP
New	**SHM-43**	0.01	35 ns	5 ns	1 ps	150	5 µV/µs	24-Pin DIP
New	**SHM-49**	0.01	140 ns	6 ns	15 ps	16	1 µV/µs	8-Pin DIP
	SHM-45	0.01	200 ns	6 ns	±50 ps	16	0.5 µV/µs	24-Pin DIP
	SHM-4860	0.01	200 ns	6 ns	±50 ps	16	0.5 µV/µs	24-Pin DIP
	SHM-30	0.01	500 ns	-25 ns	0.1 ns	4.5	0.01 µV/µs	14-Pin DIP
	SHM-20	0.01	1 µs	30 ns	1 ns	2	0.8 µV/µs	14-Pin DIP
	SHM-91	0.003	2 µs	15 ns	300 ps	2	5 µV/µs	24-Pin DIP
New	**SHM-945**	0.0004	500 ns	5ns	10 ps	12	0.5 µV/µs	24-Pin DIP
Advanced	**MSH-840***	0.01	750 ns	6 ns	±1 ns	1	1 µV/µs	32-Pin DIP

* QUAD Simultaneous Sample-Hold with 4-Channel Multiplexer

HYBRID DATA ACQUISITION SYSTEMS

	Model	Resolution (Bits)	Throughput (KHz)	Linearity Error (Max)	Power (Watts Max)	Channels	Case
	HDAS-16	12	50	±3/4 LSB	1.75	16 SE	62-Pin
	HDAS-8	12	50	±3/4 LSB	1.75	8 DE	62-Pin
	HDAS-75	12	75	±3/4 LSB	0.7	8 SE	40-Pin DIP
	HDAS-76	12	75	±3/4 LSB	0.7	4 DE	40-Pin DIP
	HDAS-534	12	250	±3/4 LSB	3.0	4 DE	40-Pin DIP
	HDAS-538	12	250	±3/4 LSB	3.0	8 SE	40-PIN DIP
	HDAS-524	12	400	±3/4 LSB	3.0	4 DE	40-Pin DIP
	HDAS-528	12	400	±3/4 LSB	3.0	8 SE	40-Pin DIP
Preliminary	**HDAS-950**	16	100	±1/2 LSB @ 14 BITS	1.4	8 SE	40-Pin DIP
Preliminary	**HDAS-951**	16	100	±1/2 LSB @ 14 BITS	1.4	4 DE	40-Pin DIP

MULTIPLEXERS

	Model	Channels	Settling Time 20V to 0.01%	Access Time	Input Range	Power (Watts)	Case
	MXD-409	4 D	3 µs	500 ns	±15V	0.105	16-Pin DIP
	MX-808	8 SE	3 µs	500 ns	±15V	0.105	16-Pin DIP
	MXD-807	8 D	3 µs	500 ns	±15V	0.105	28-Pin DIP
	MX-1606	16 SE	3 µs	500 ns	±15V	0.105	28-Pin DIP
	MVD-409	4 D	2.8 µs	350 ns	±15V	0.055	16-Pin DIP
	MV-808	8 SE	2.8 µs	350 ns	±15V	0.055	16-Pin DIP
	MVD-807	8 D	2.4 µs	300 ns	±15V	0.105	28-Pin DIP
	MV-1606	16 SE	2.4 µs	300 ns	±15V	0.105	28-Pin DIP
	MX-818C	8 SE/4D	800 ns	125 ns	±15V	0.540	18-Pin DIP
	MX-1616C	16 SE/8 D	800 ns	150 ns	±15V	0.900	28-Pin DIP
New	**MX-826**	8 SE	200 ns	70 ns	±10.5V	0.395	24-Pin DIP
New	**MX-850**	4 SE	50 ns	20 ns	±10V	0.250	14-Pin DIP

OPERATIONAL AMPLIFIERS

Model	DC Open Loop Gain (V/V)	Settling Time (µsec)	Slew Rate (V/µsec)	Gain Bandwidth (MHz)	Case
AM-500	10^6	200 ns/0.01%	1000	100	14-Pin DIP
AM-1435	10^5	70 ns/0.01%	300	1000	14-Pin DIP

INSTRUMENTATION AMPLIFIERS

Model	Gain Range	Settling Time	Case
AM-551	1 to 1000	2 µs/0.01%	16-Pin DIP

RESISTOR TUNEABLE OSCILLATORS

Model	Frequency Range	Accuracy	Case
ROJ-20	20 Hz to 20 KHz	0.5% @ 1 KHz	24-pin DIP
ROJ-1K	1KHz to 100 KHz	0.5% @ 10 KHz	24-pin DIP

TUNABLE ACTIVE FILTERS

Model	Poles	Low Pass	High Pass	Band Pass	Band Reject	Rolloff (dB/Oct)	Frequency Cutoff Range (FC)	Filter Type	Gain	Case
FLT-DL41 *	4	♦				30	100 to 400KHz	CA	+1	32 DIP
FLT-DL42 *	4	♦				30	250 to 1000 KHz	CA	+1	32 DIP
FLT-DL51 *	5	♦				50	120 to 470 KHz	CA	+1	32 DIP
FLT-DL52 *	5	♦				50	300 to 1200KHz	CA	+1	32 DIP
FLT-DL41/DL51 § *	7	♦				50	100 to 400KHz	CA	+1	2-32 DIP
FLT-DL42/DL52 § *	7	♦				50	0.25 to 1.0MHz	CA	+1	2-32 DIP
FLT-C1	7	♦				52	78 Hz-20 KHz	CH	1, 2, 4, 8	32 DIP
FLJ-DC	2	♦	♦	♦	♦	12	1 Hz-159 KHz	BU,CH,BE	1 ~ 10	40 QDIP
FLJ-D1	2	♦	♦	♦	♦	12	1 Hz-1.599 KHz	BU	1 ~ 10	40 QDIP
FLJ-D2	2	♦	♦	♦	♦	12	100 Hz-159.9 KHz	BU	1 ~ 10	40 QDIP
FLJ-D5LA1	5	♦				60	10 Hz-2 KHz	CA	0 ±0.3 dB max	40 QDIP
FLJ-D5LA2	5	♦				60	100 Hz-20 KHz	CA	0 ±0.3 dB max	40 QDIP
FLJ-D6LA1	6	♦				80	10 Hz-2 KHz	CA	0 ±0.3 dB max	40 QDIP
FLJ-D6LA2	6	♦				80	100 Hz-20 KHz	CA	0 ±0.3 dB max	40 QDIP
FLJ-VB	2			♦		12	200Hz-20KHz	BU	±1dB	40 QDIP
FLJ-VH	4		♦			24	20Hz-20KHz	BU	±0.5dB	40 QDIP
FLJ-VL	4	♦				24	100Hz-100KHz	BU	±0.5dB	40 QDIP
FLJ-R3BA1	3			♦		—	10Hz-2KHz	CA	0 ±1dB max	40 QDIP
FLJ-R3BA2	3			♦		—	100Hz-20KHz	CA	0 ±1dB max	40 QDIP
FLJ-R8LA1	8	♦				135	10Hz-2KHz	CA	0 ±0.1dB max	40 QDIP
FLJ-R8LA2	8	♦				135	100Hz-20KHz	CA	0 ±0.1dB max	40 QDIP
FLJ-R8LB1	8	♦				100	10Hz-2KHz	CA	0 ±0.1dB max	40 QDIP
FLJ-R8LB2	8	♦				100	100Hz-20KHz	CA	0 ±0.1dB max	40 QDIP
FLJ-UR1BA1	1			♦		—	40Hz-1.6KHz	BU	0 ±1dB	20 SIP
FLJ-UR2BA1	2			♦		- -	40Hz-1.6KHz	BU	0 ±1dB	20 SIP
FLJ-UR2EA1	2				♦	—	40Hz-1.6KHz	BU	0 ±0.3dB	20 SIP
FLJ-UR2LH1	2	♦	♦			12	40Hz-1.6KHz	BU	0 ±0.3dB	20 SIP
FLJ-UR4HA1	4		♦			24	40Hz-1.6KHz	BU	0 ±1dB	20 SIP
FLJ-UR4HB1	4		♦			42	40Hz-1.6KHz	CH	0 ±1dB	20 SIP
FLJ-UR4LA1	4	♦				24	40Hz-1.6KHz	BU	0 ±0.3dB	20 SIP
FLJ-UR4LB1	4	♦				42	40Hz-1.6KHz	CH	0 ±0.3dB	20 SIP
FLJ-UR1BA2	1			♦		—	400Hz-10KHz	BU	0 ±1dB	20 SIP
FLJ-UR2BA2	2			♦		- -	400Hz-10KHz	BU	0 ±1dB	20 SIP
FLJ-UR2EA2	2				♦	—	400Hz-10KHz	BU	0 ±0.3dB	20 SIP
FLJ-UR2LH2	2	♦	♦			12	400Hz-20KHz	BU	0 ±0.3dB	20 SIP
FLJ-UR4HA2	4		♦			24	400Hz-5KHz	BU	0 ±1dB	20 SIP
FLJ-UR4HB2	4		♦			42	400Hz-5KHz	CH	0 ±1dB	20 SIP
FLJ-UR4LA2	4	♦				24	400Hz-20KHz	BU	0 ±0.3dB	20 SIP
FLJ-UR4LB2	4	♦				42	400Hz-20KHz	CH	0 ±0.3dB	20 SIP
FLT-U2	2	♦	♦	♦		12	0.001Hz-200KHz	BU,CH,BE,CA	0.1-1000	16 DIP

BU = Butterworth BE = Bessel
CH = Chebyshev CA = Cauer/Elliptical

All Filters operate over the commercial temperature range -20°C to +70°
Model FLT-U2 also operates at -55°C to +125°C
§ Cascaded Pair * Preliminary

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